CPE201
Digital Design

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Class 18: Flip-Flops

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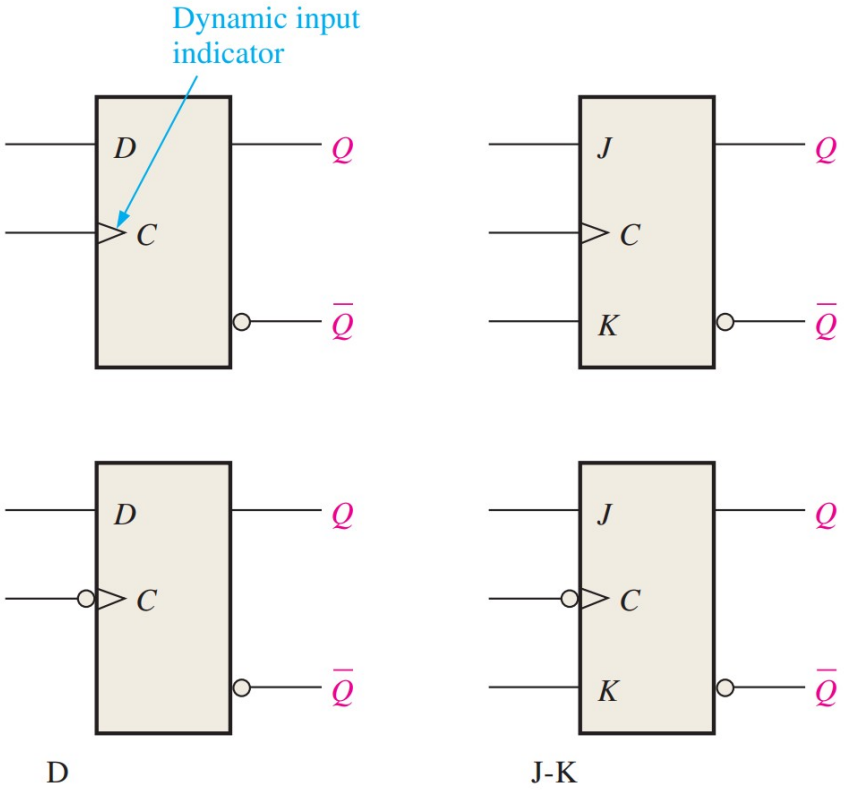
Vocabulary

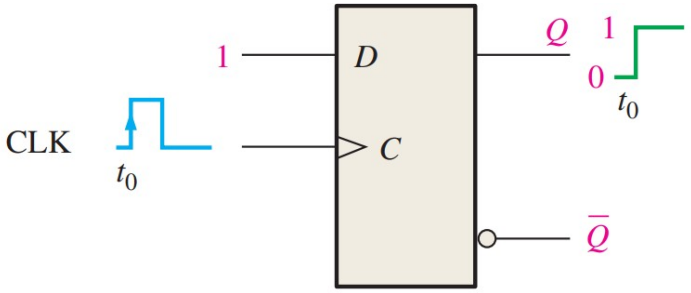
- Bistable Multivibrator
  - 2 States
- Synchronous
  - There is a clock
- Clock
  - Signal that alternates H/L at a set interval

Vocab

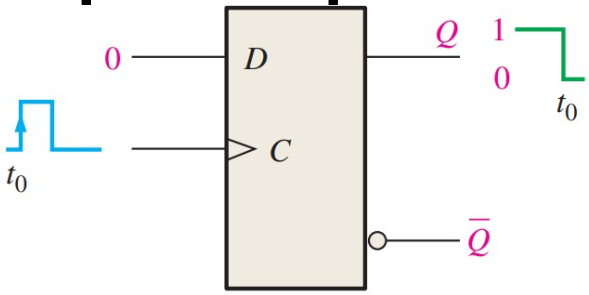
- Edge Triggered
  - State changes on edg
  - Positive or rising edg
  - Negative or falling ed



D Flip-Flop



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



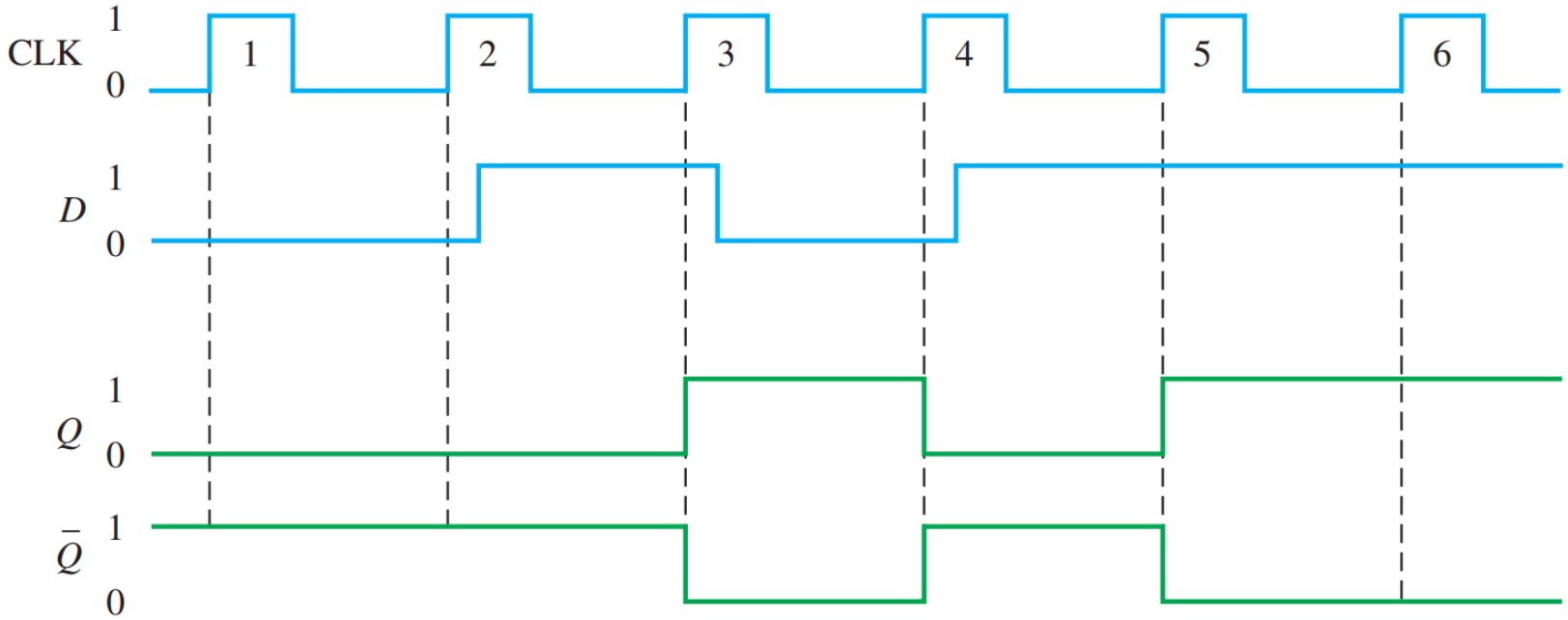
(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

Truth table for a positive edge-triggered D flip-flop.

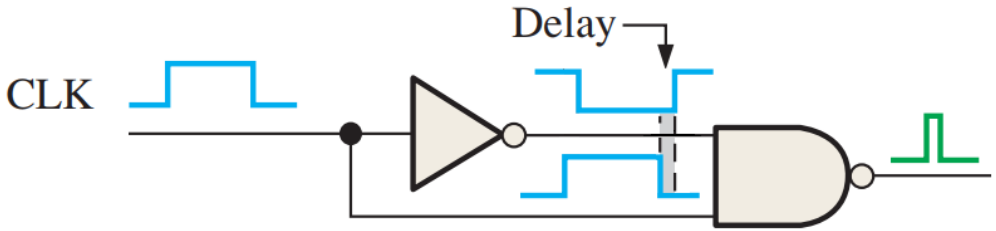
Inputs		Outputs		
D	**CLK**	***Q***	$\overline{Q}$	**Comments**
0	↑	0	1	RESET
1	↑	1	0	SET

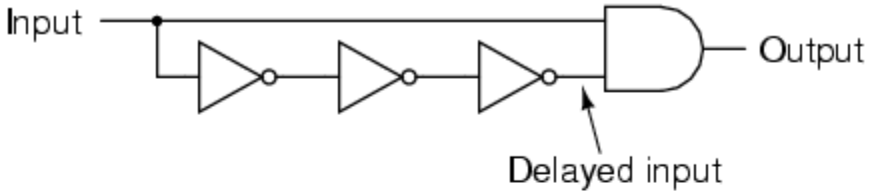
↑ = clock transition LOW to HIGH

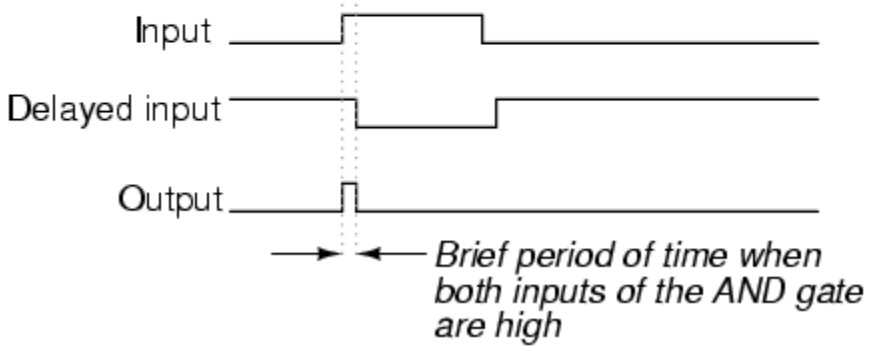
Example



Edge Detection

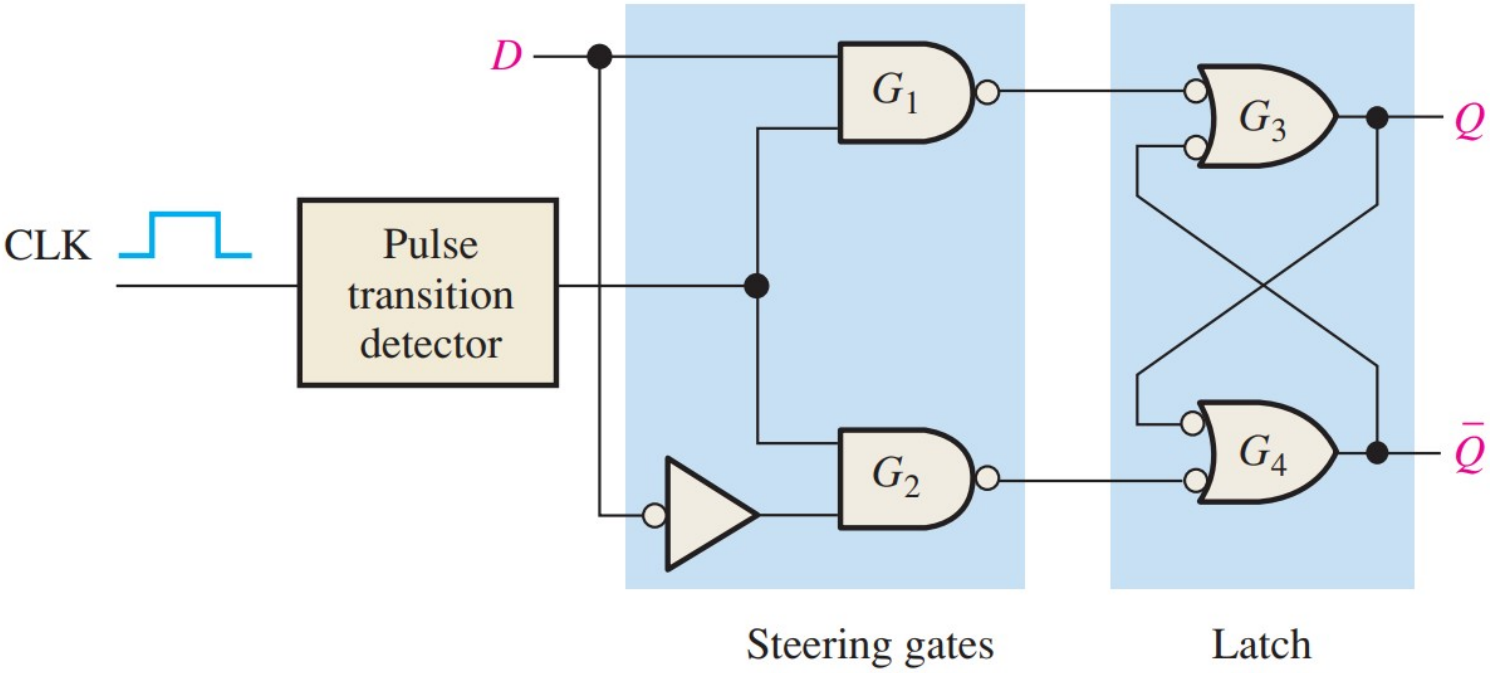




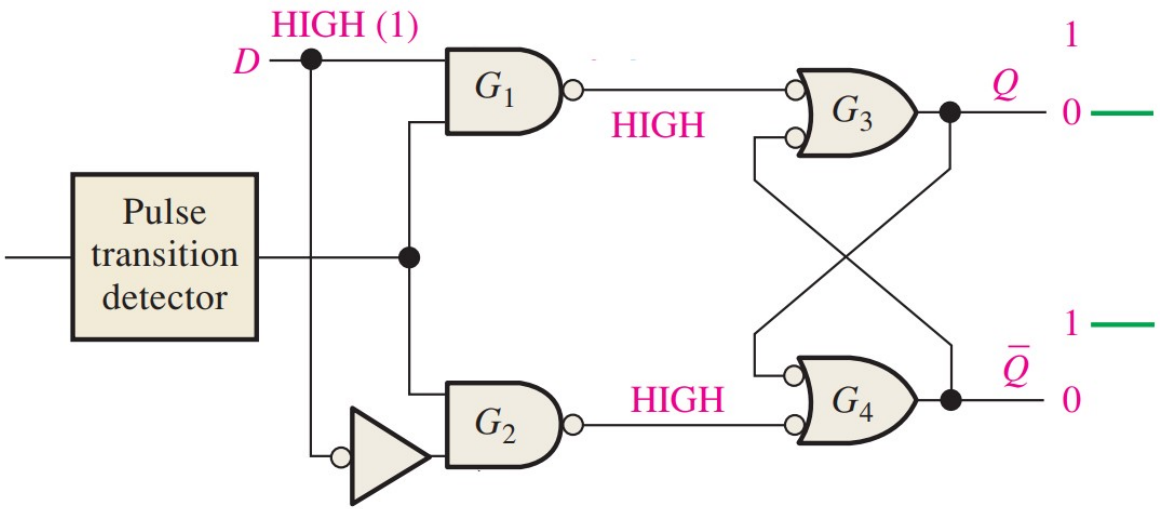


Circuit

- G_3 and G_4 are NANDs (like from latches)



Circuit Walkthrough

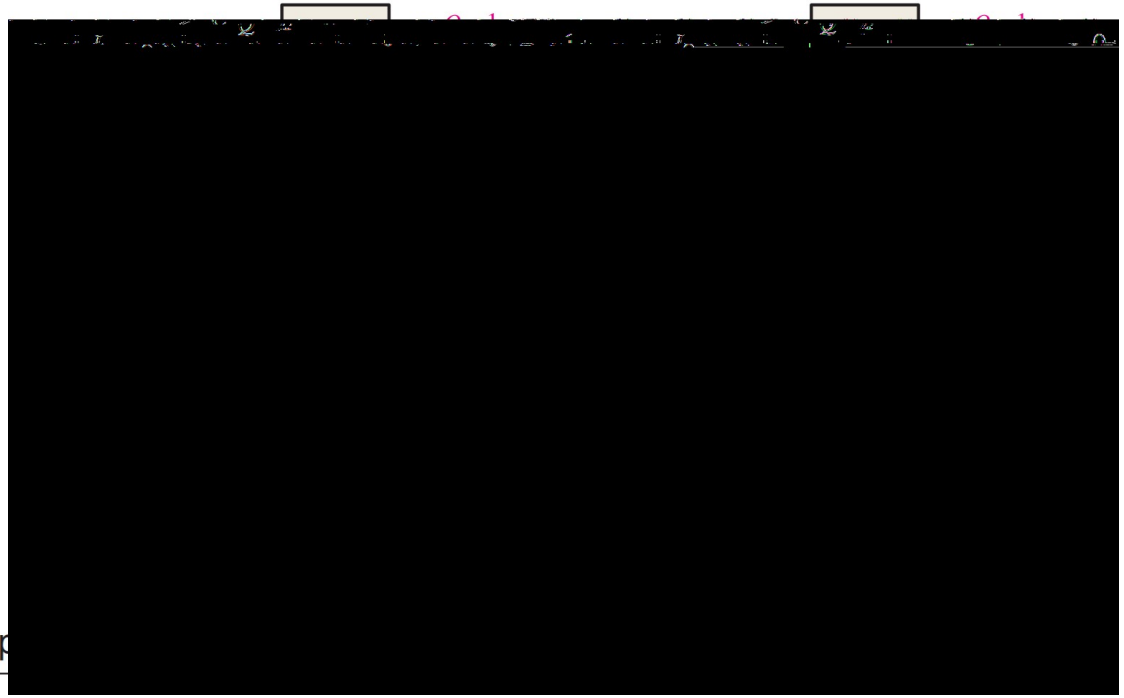


Truth table for a 2-input NAND gate.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	1
1	0	1
1	1	0

J-K Flip-Flop

- S-R Latch+



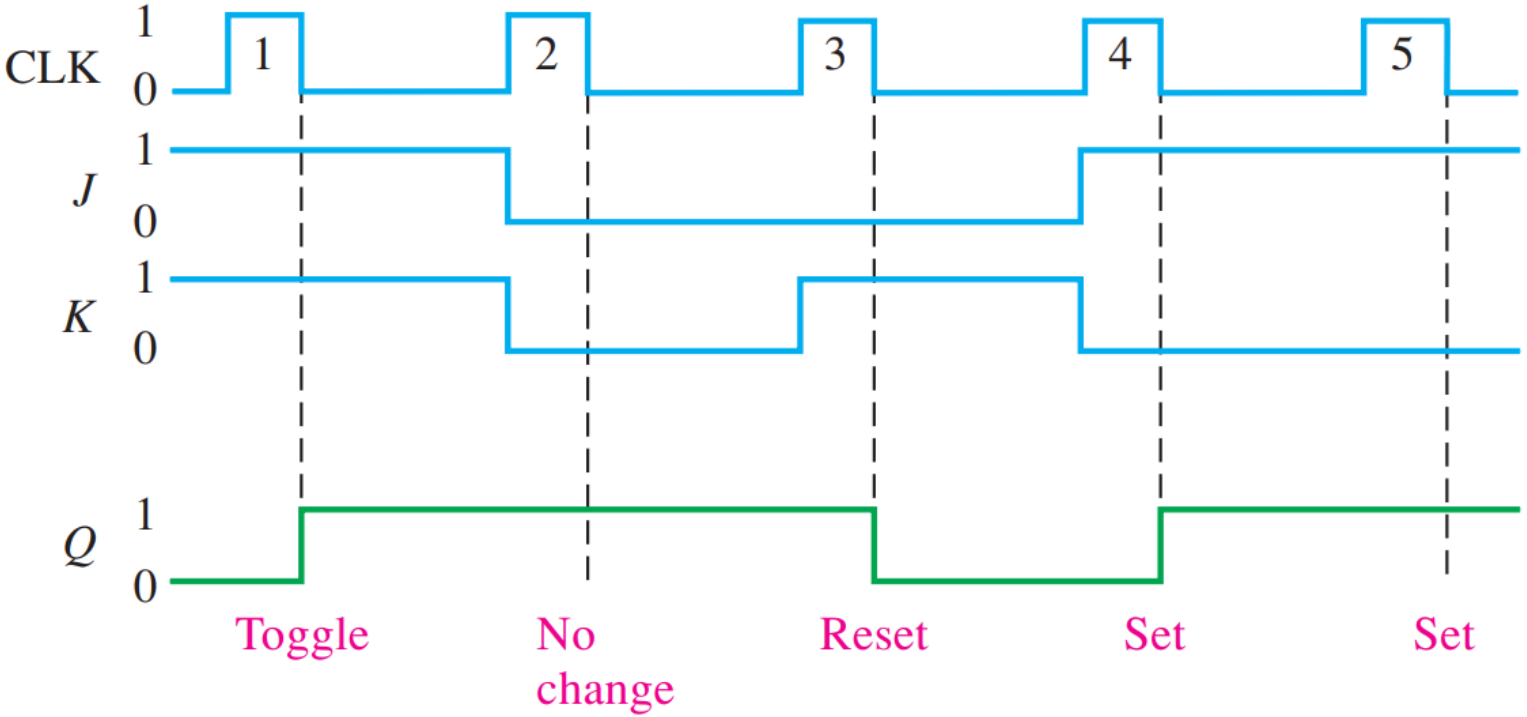
Truth table for a positive edge-triggered J-K flip-flop

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

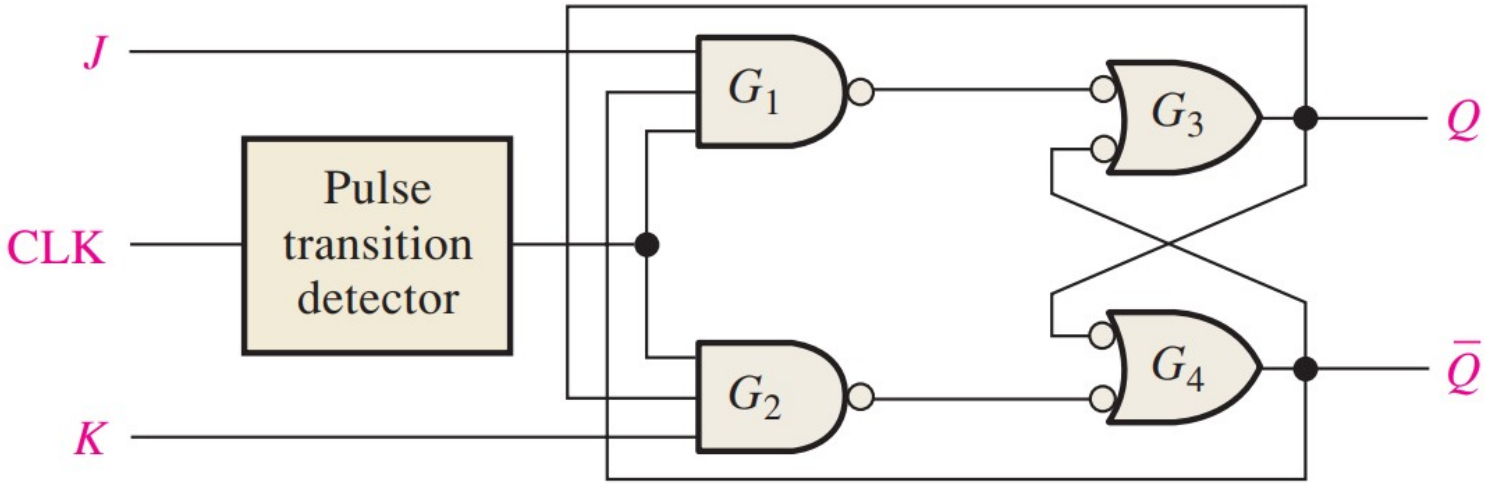
↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

Example



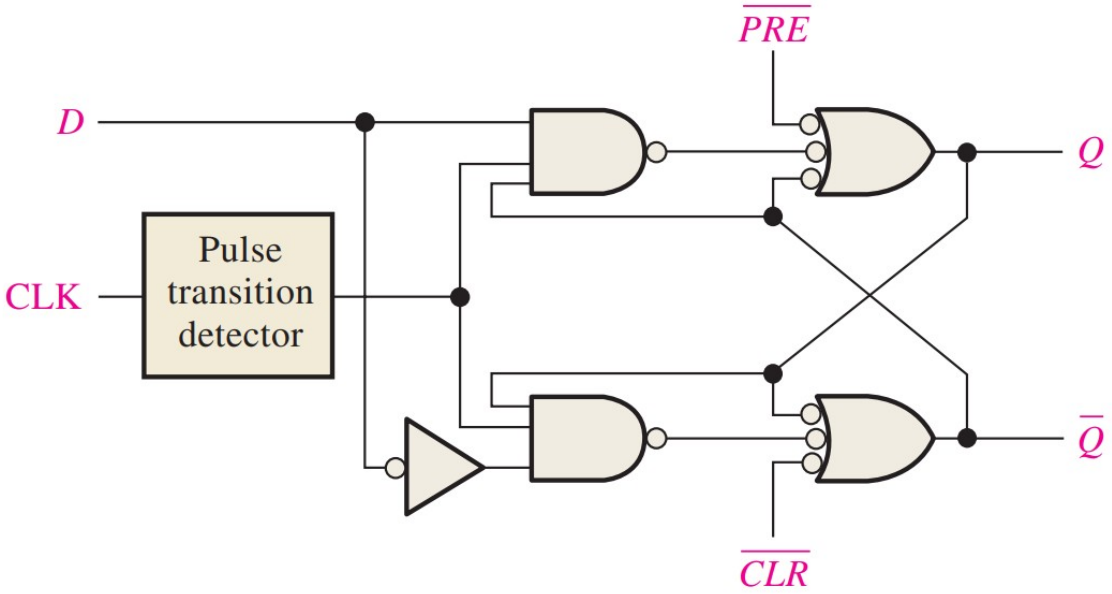
Circuit

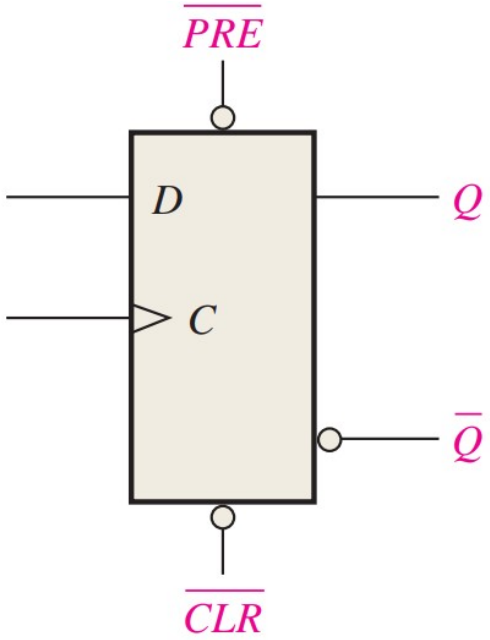


Asynchronous Set and Reset

- Independent on clock
  - Initialization on startup
  - Override
- Also called Preset and Clear

Circuit

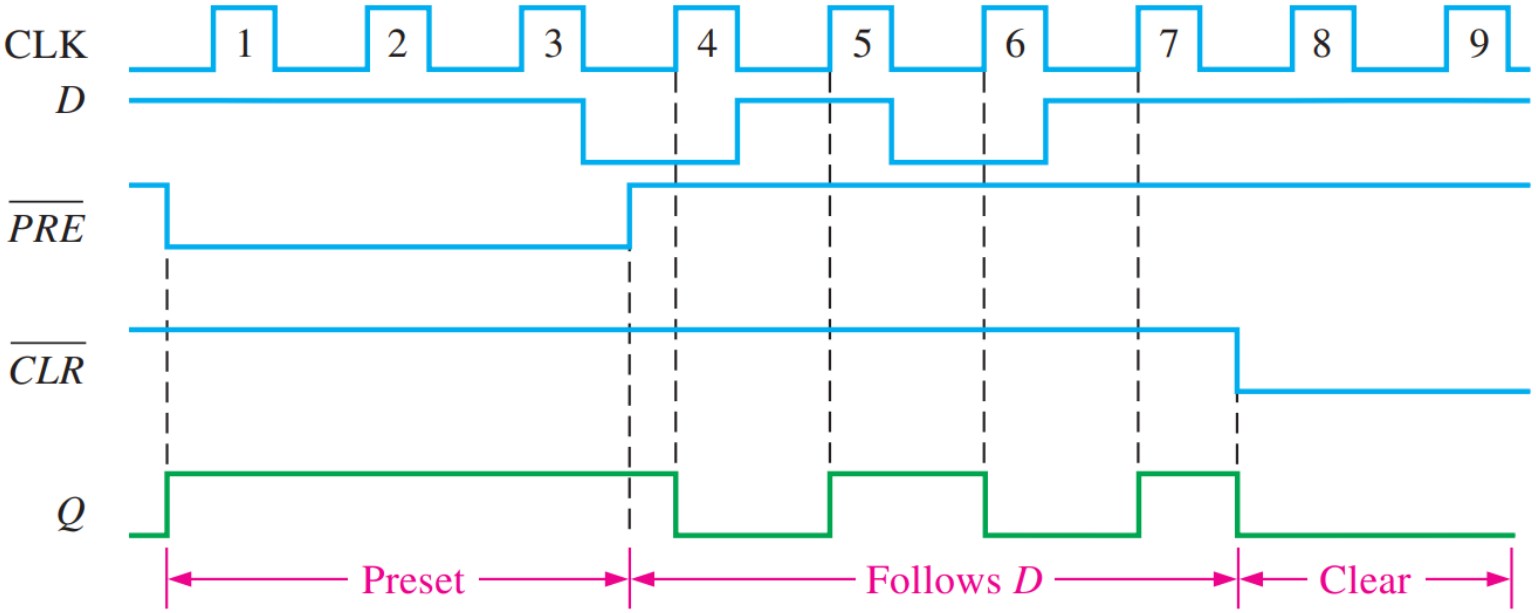




Preset and Clear

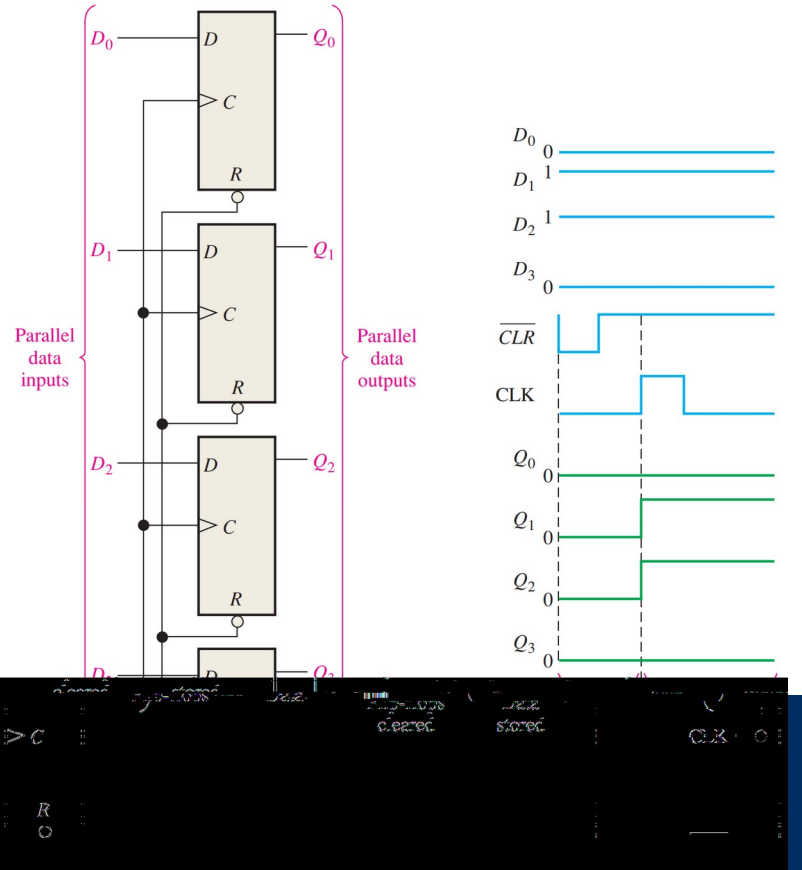
- Reaches into the Latch portion of the circuit
- Can also be done in J-K Flip-Flop
- Active Low inputs
  - Normal operation is both high
  - Both low creates latch invalid state

Example



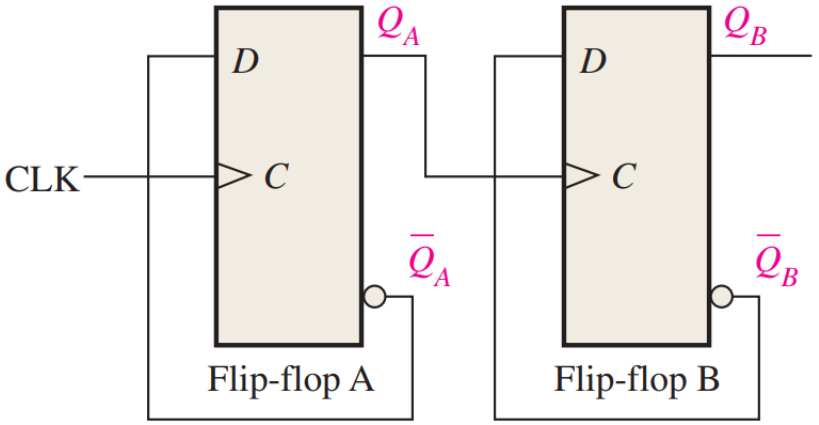
Application – Data Storage

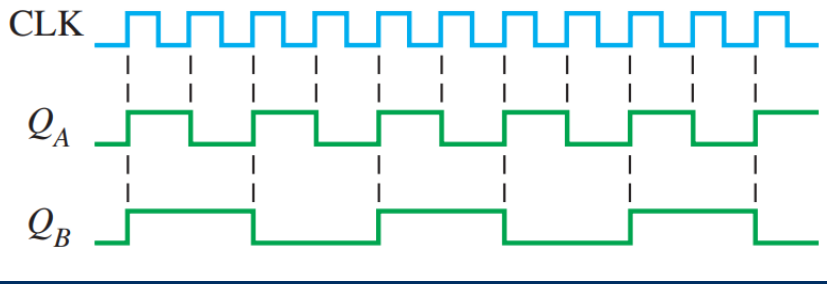
- Parallel storage
- Data on lines stored at each clock
- Covered more later



Application - Frequency Division

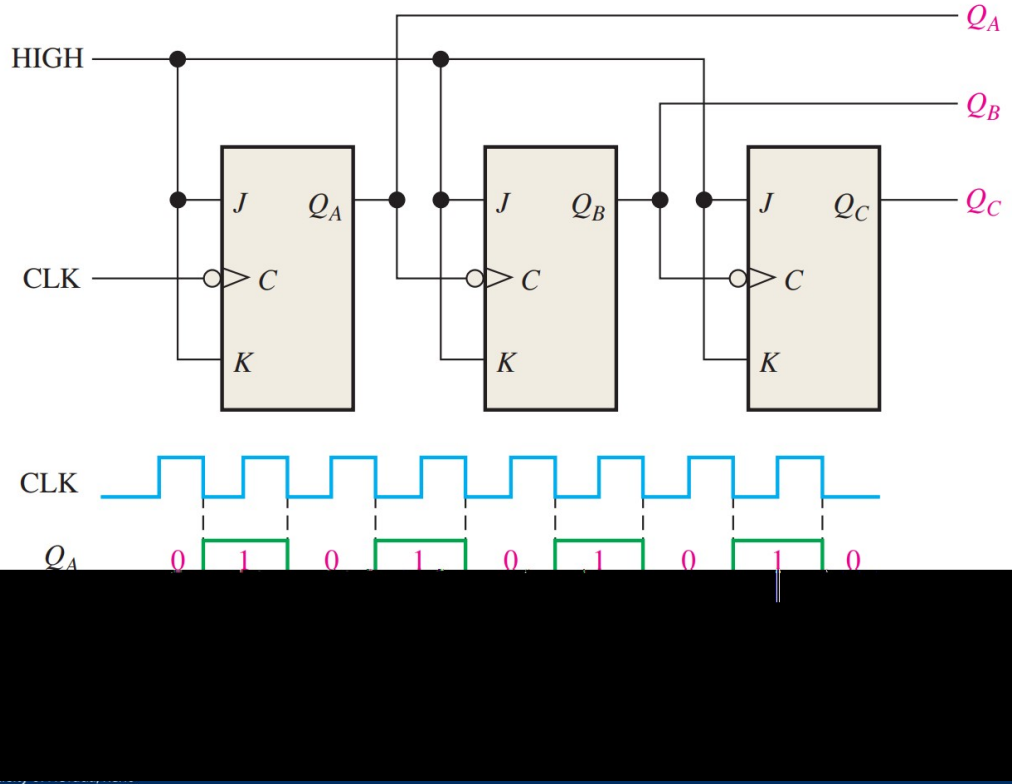
- Divide by 2
- Good for running multiple subsystems



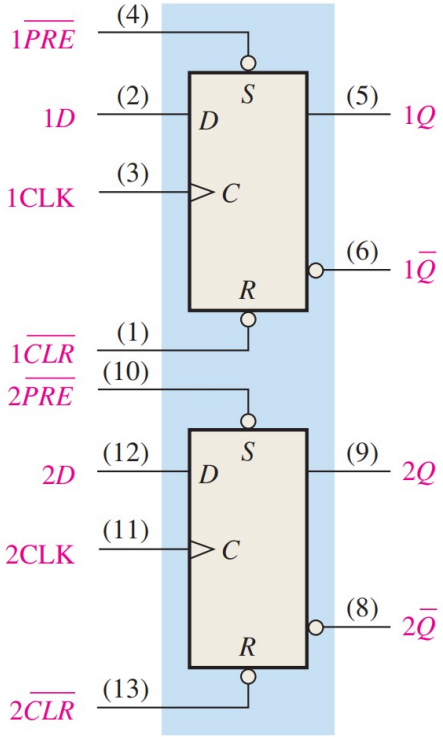


Application - Counting

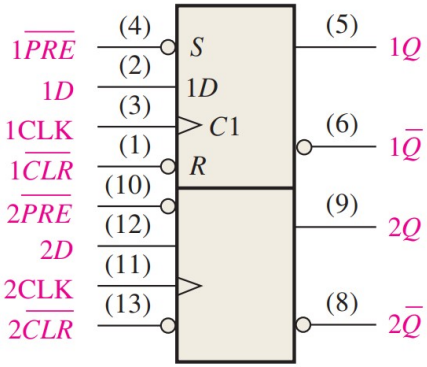
- Like freq division
- Line up the divisic
  to count in binary
- Counts clock cycle
- J-Ks instead of Ds



Real Chips – 74HC74 and 74HC112

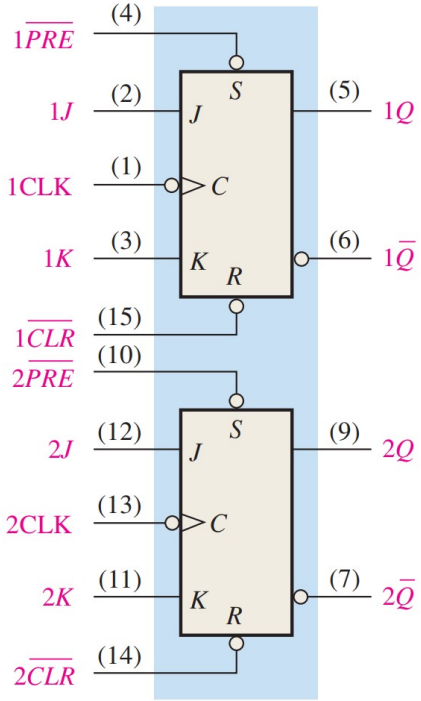


Individual logic symbols

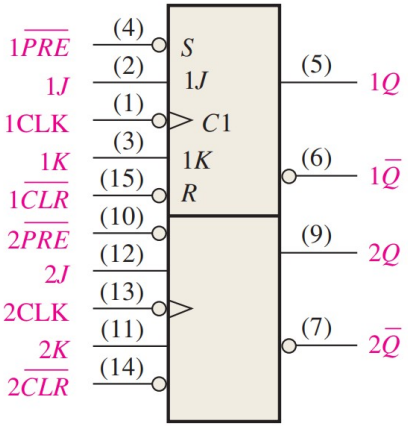


Single block logic symbol

Note: The S and R inside the block indicate that $\overline{PRE}$ SETS and $\overline{CLR}$ RESETS.



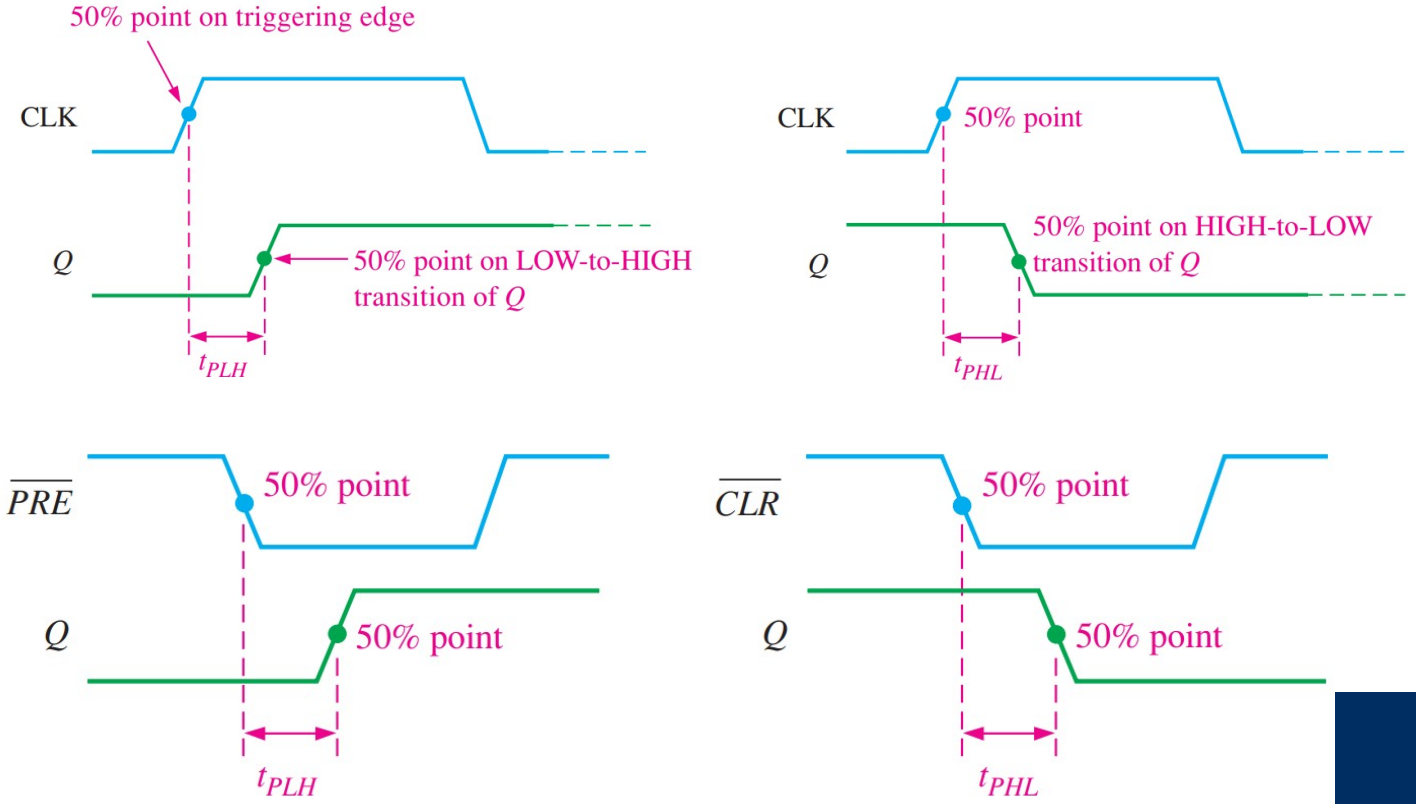
Individual logic symbols



Single block logic symbol

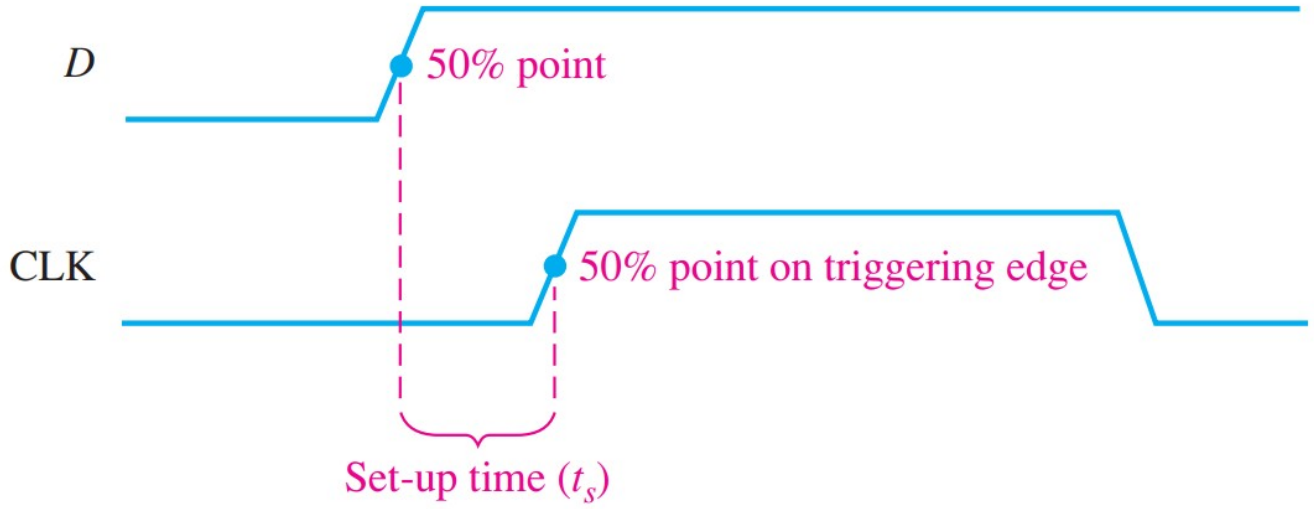
The 74HC112 dual negative edge-triggered J-K flip-flop.

Propagation Delays



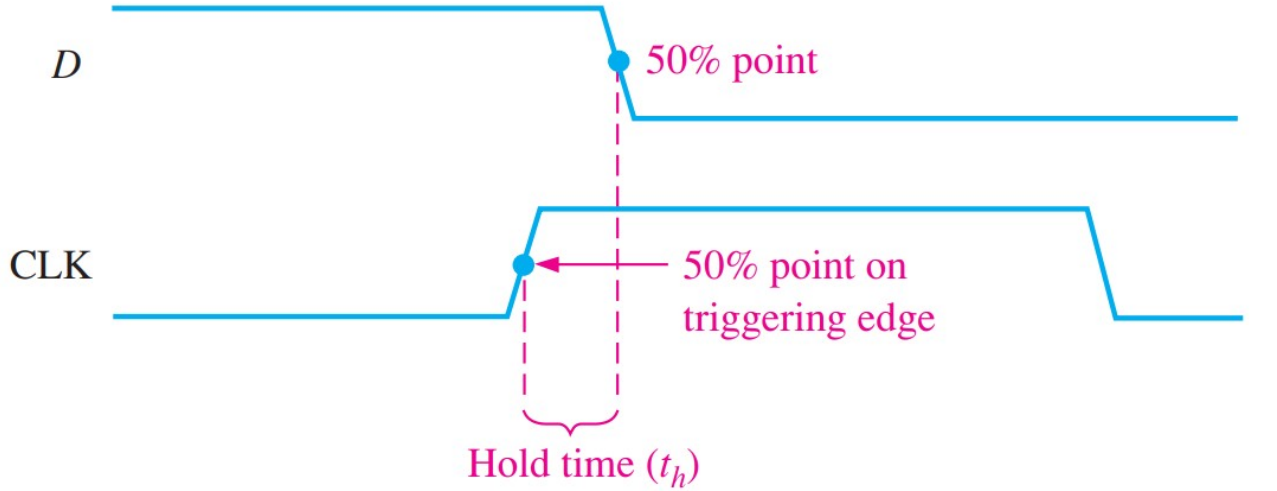
Setup Time

- Data time on the line BEFORE clocking it in



Hold Time

- Data time on the line AFTER clocking it in



Reading

- This lecture
  - Sections 7.2-7.4
- Next lecture
  - Sections 7.5-7.7