

Answer all questions completely. Put a box around the final solution. Put your name on it. Show your work.

By hand:

- Given the asynchronous ripple counter in Figure 1, give the output waveforms for Q_0 , Q_1 , and Q_2 for 16 clock cycles.

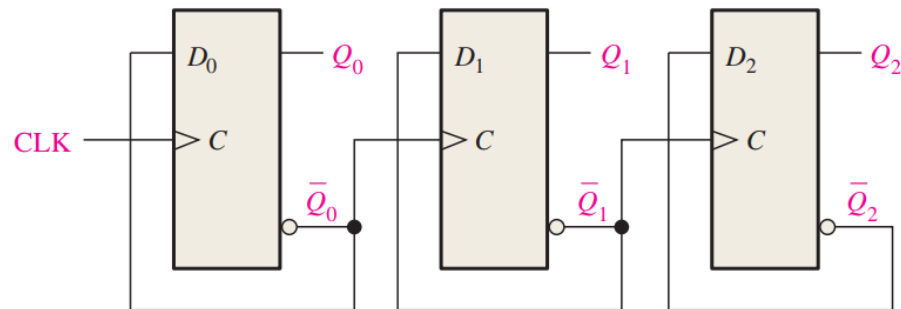


Figure 1

Clock	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Q2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Q1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
Q0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

- Using the asynchronous ripple counter in Figure 1 and assuming that the propagation delay from an input clock to a change in the output of Q is 9ns, what is the worst-case delay (i.e. longest delay) between an input clock pulse and the counter being in a final state. Give which state(s) of the counter have the worst-case delay.

The worst case delay is when the last bit (Q_2) has to change, that is when the propagation delay to the final output has to ripple through all 3 FFs. The longest delay will be $3 \times 9\text{ns} = 27\text{ns}$. This will happen on the change from 011 to 100 and from 111 to 000.

- If the counter from Problem 2 was synchronous, what would the worst cast propagation delay be?

The worst case for a synchronous counter is always only one propagation delay time = 9ns.

- Give the block diagrams of cascaded counters to give the following frequencies using a 10MHz clock and only Mod 5 counters, decade counters, and single flip-flops

a. 2.5MHz

$10\text{MHz}/2.5\text{MHz} = 4$, so we need a divisor of 4 to get the clock speed we want.

The clock has to go through 2 single flip-flops = $2 * 2 = 4$

b. 40kHz

$10\text{MHz}/40\text{kHz} = 250$, so we need a divisor of 250 to get the clock speed we want.

The clock has to go through one decade counter and 2 Mod 5 counters = $10 * 5 * 5 = 250$

The 3 counters can be in any order.

c. 250kHz

$10\text{MHz}/250\text{kHz} = 40$, so we need a divisor of 40 to get the clock speed we want.

The clock has to go through one decade counter and 2 single flip-flops = $10 * 2 * 2 = 4$

The clock could also go through one Mod 5 counter and 3 single flip-flops = $5 * 2 * 2 * 2 = 40$

The counters/flip-flops can be in any order.

5. Given the Mod 16 counter and input waveforms in Figure 2, give the output waveforms ($Q_0 - Q_3$).

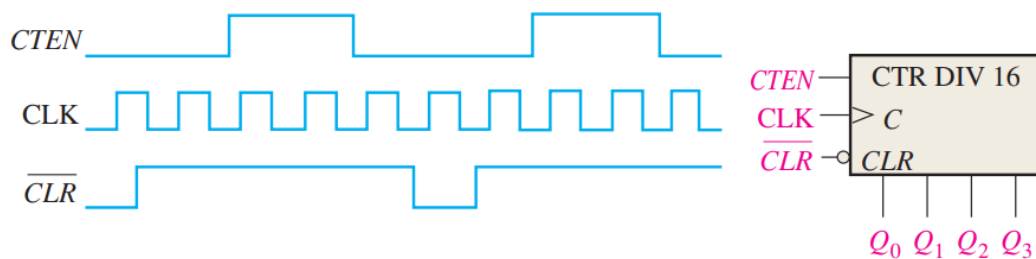


Figure 2

Clock	1	2	3	4	5	6	7	8	9	10
Q_3	0	0	0	0	0	0	0	0	0	0
Q_2	0	0	0	0	0	0	0	0	0	0
Q_1	0	0	0	1	1	0	0	0	1	1
Q_0	0	0	1	0	0	0	0	1	0	0

The count only goes up on clock 3-4 and 8-9

The count is reset on clock 6