CPE201
Digital Design

By Benjamin Haas

Class 24: Counters, Design and Applications

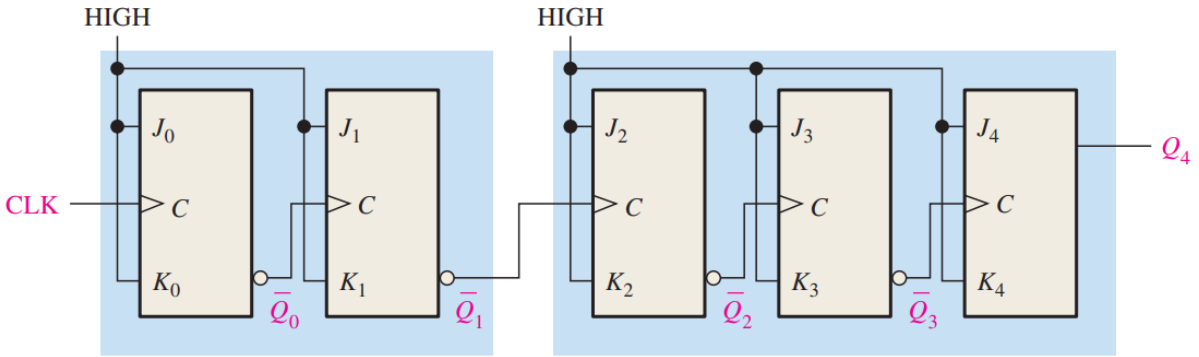
University of Nevada, Reno

Outline

- Cascading Counters
- Counter Decoding
- Counter Applications

Asynchronous Cascading

- Asynchronous is a simple cascade
  - Be wary of the time for ripple to complete

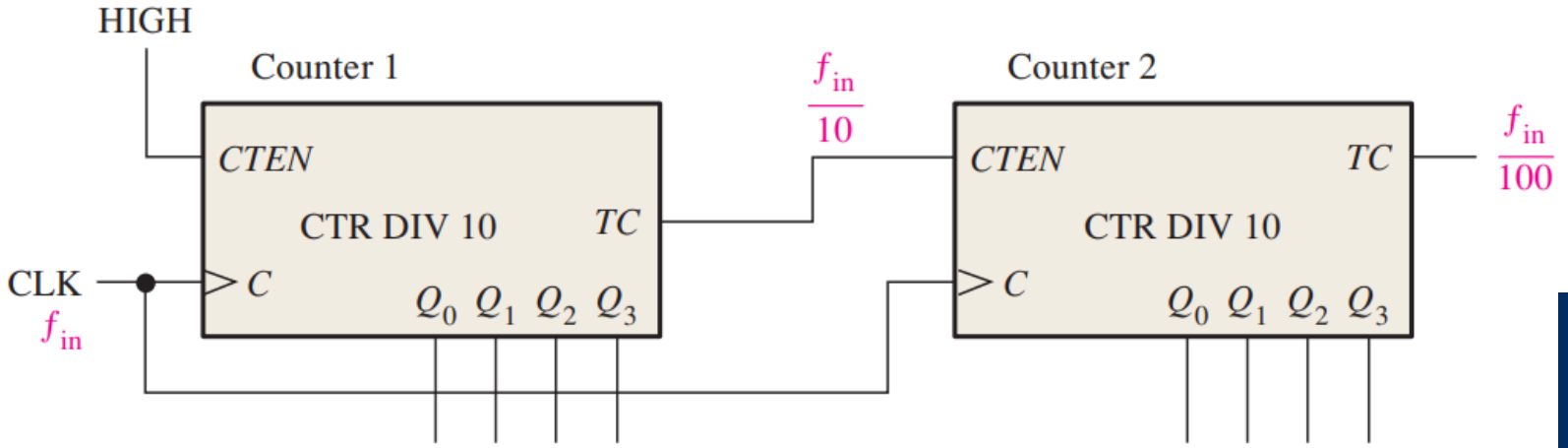


Synchronous Cascading

- Synchronous uses chip features
  - Count Enable (CTEN)
    - Lets the counter run
  - Terminal Count (TC)
    - A pulse every time the counter rolls over

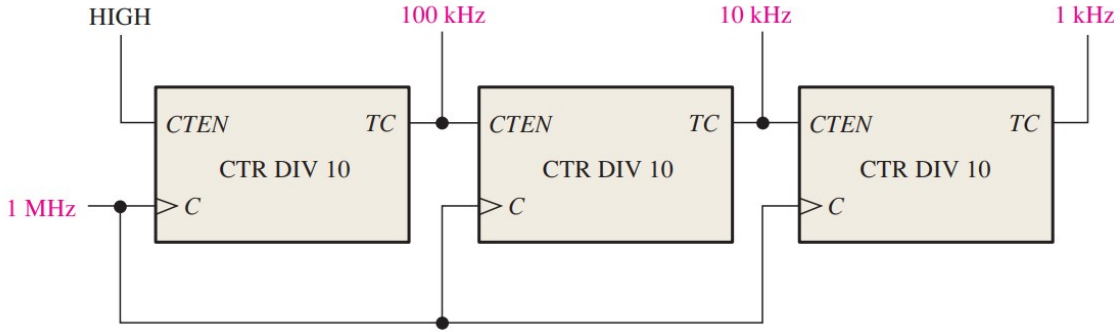
Synchronous Cascading

- Counter 2 goes up one count every time Counter 1 rolls over
  - Frequency Divider



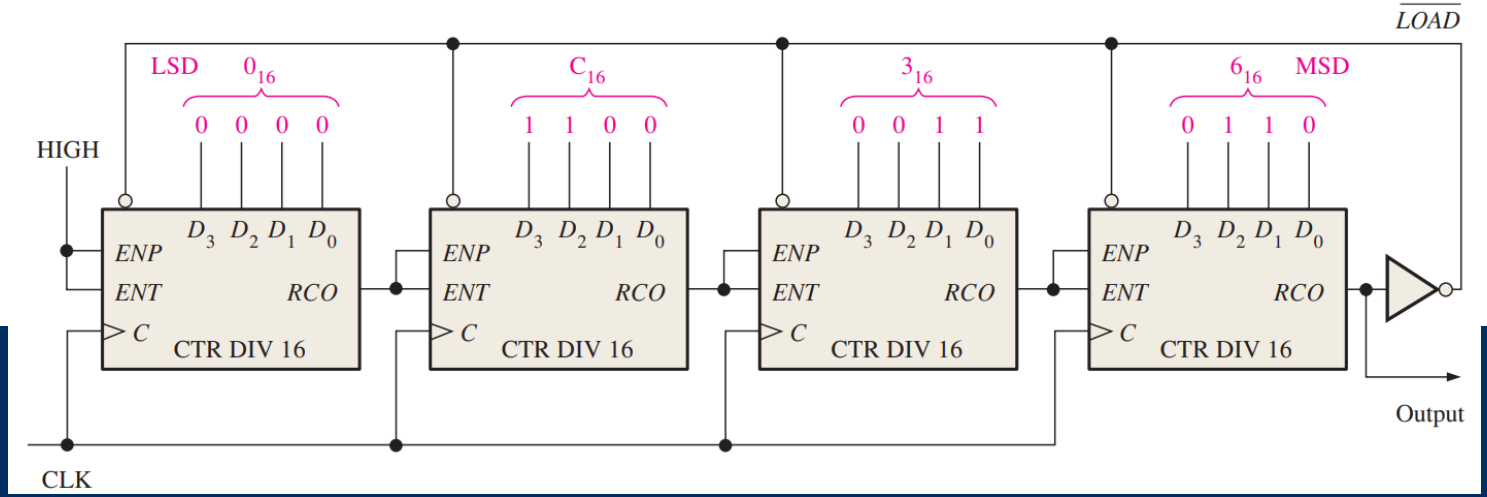
Cascading

- Multiply the mod counts to get the total
  - Can also make multiple clock frequencies



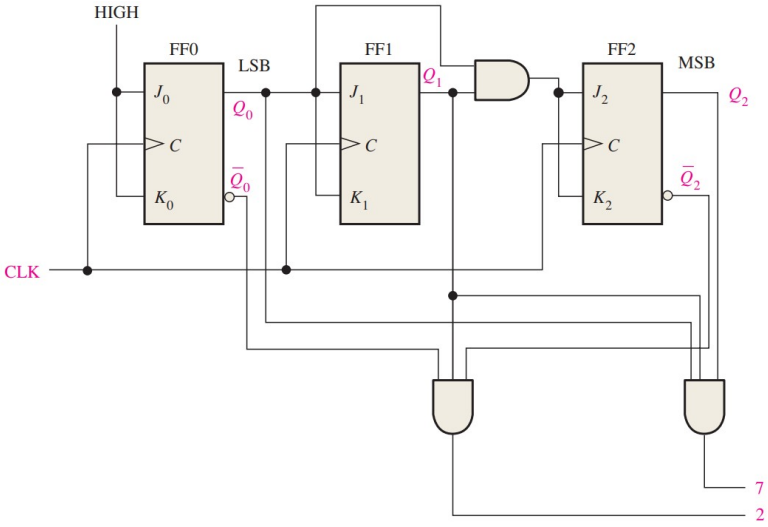
Truncated Cascading

- Use loading capability to change start value
  - Ex start at 0x63C0 = 25,536 out of
  -



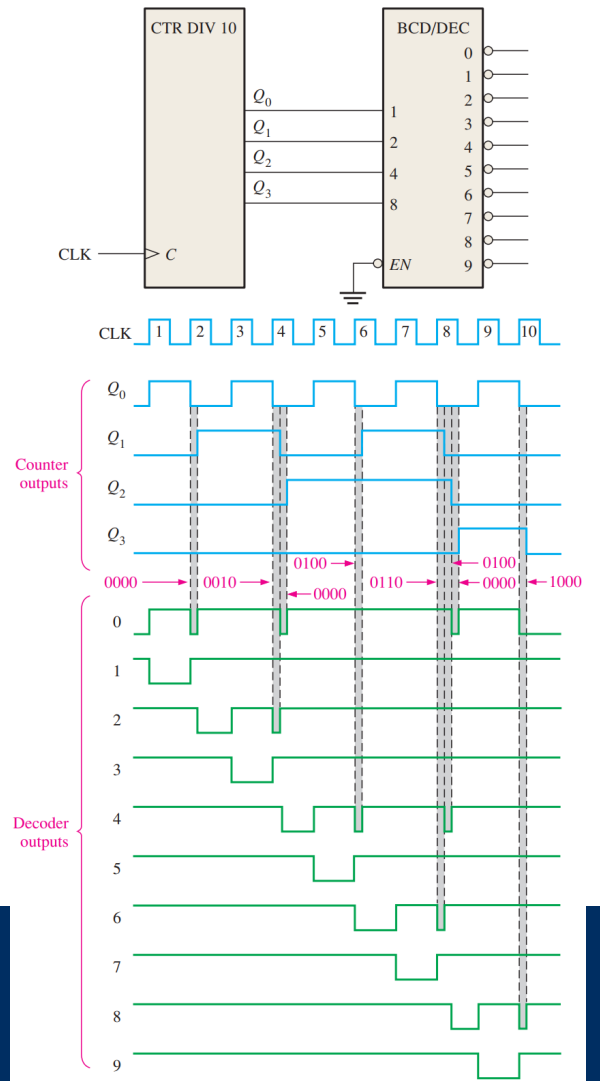
Counter Decoder

- Simple decoder
  - A pulse when the counter has a certain value
    - After data bits in a U



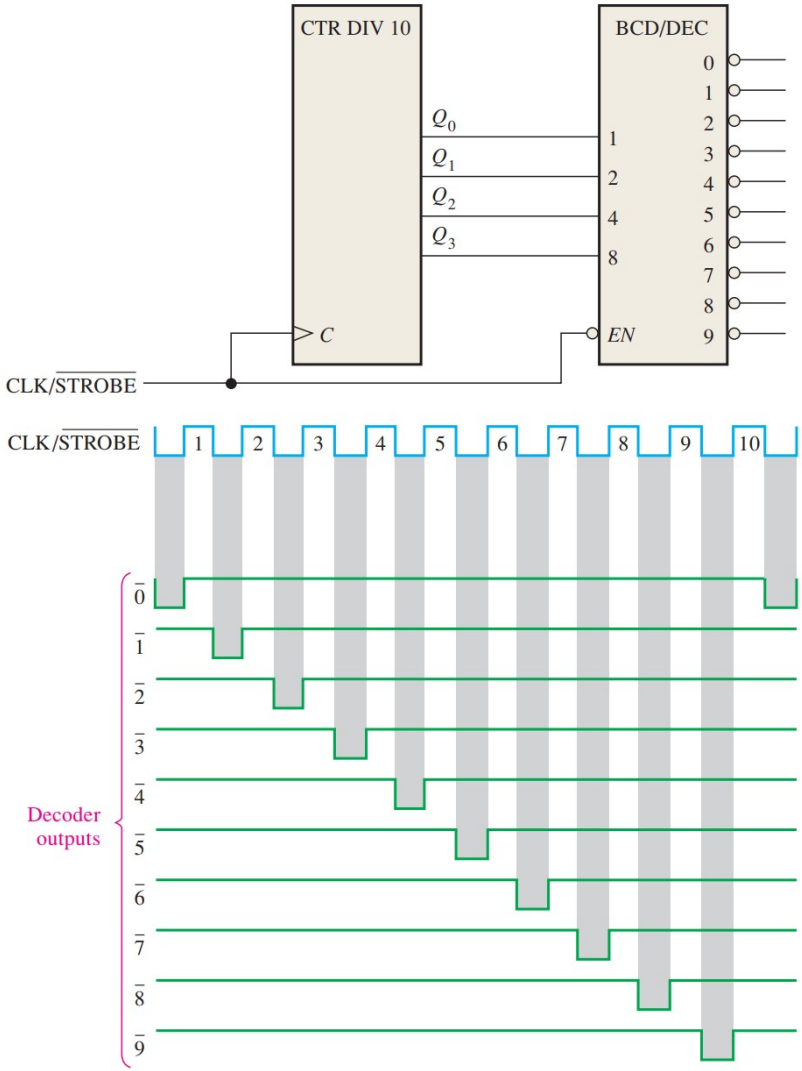
Avoid Glitches

- Sample only when the data is ready, not continuously



Strobe Inputs

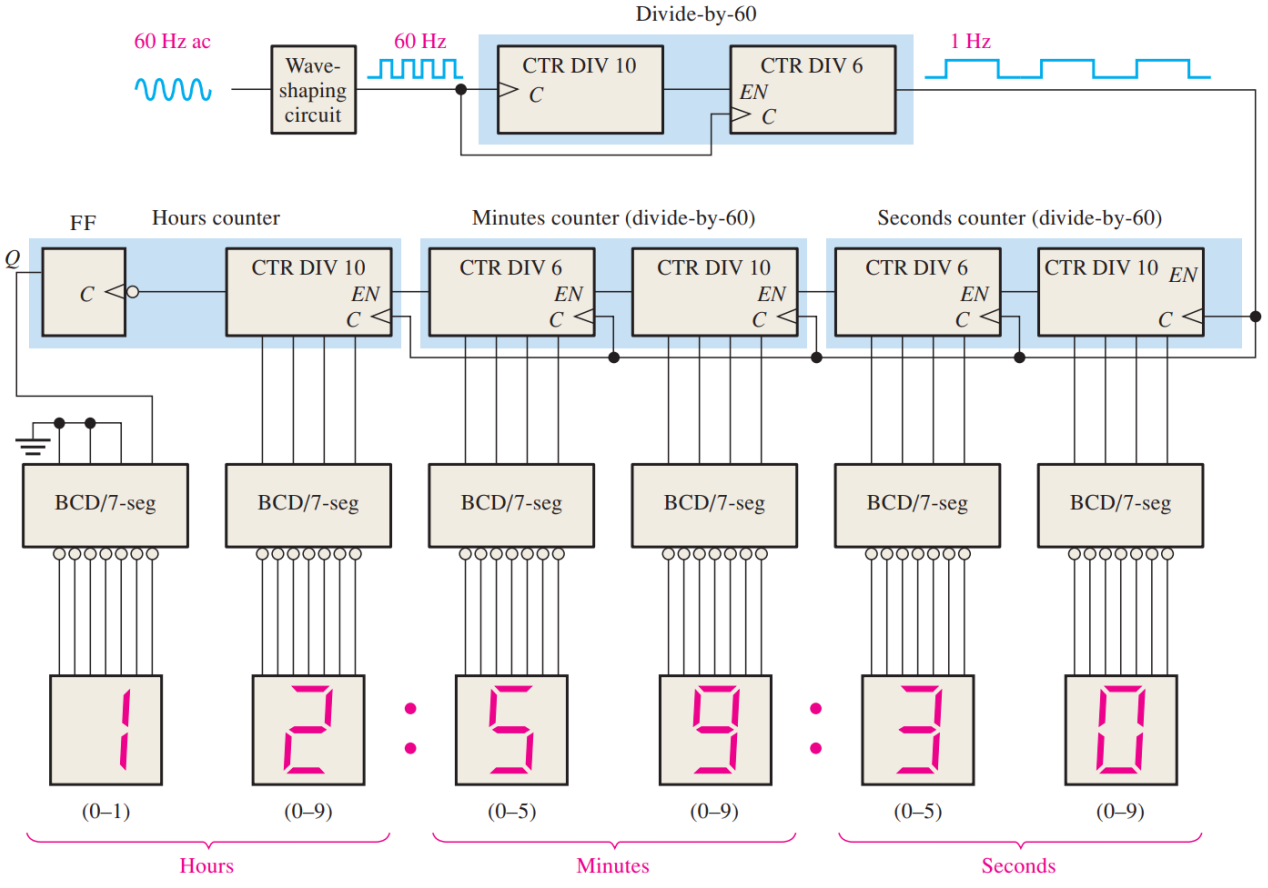
- Same concept as with MUX/DEMUX



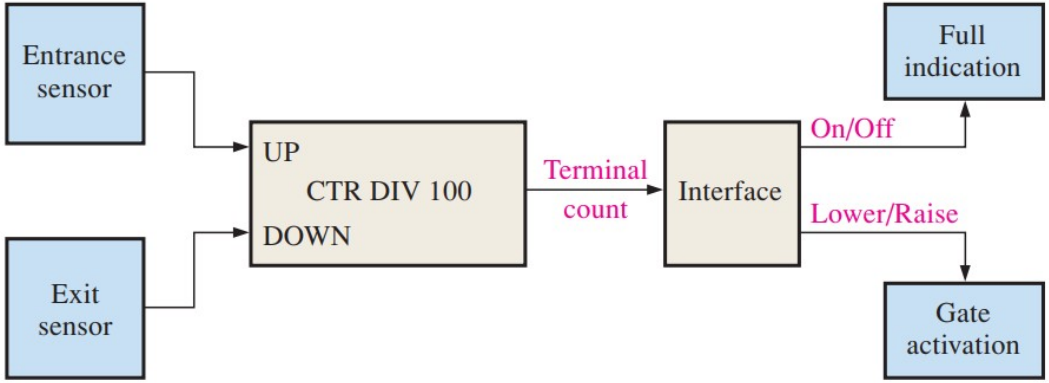
Applications

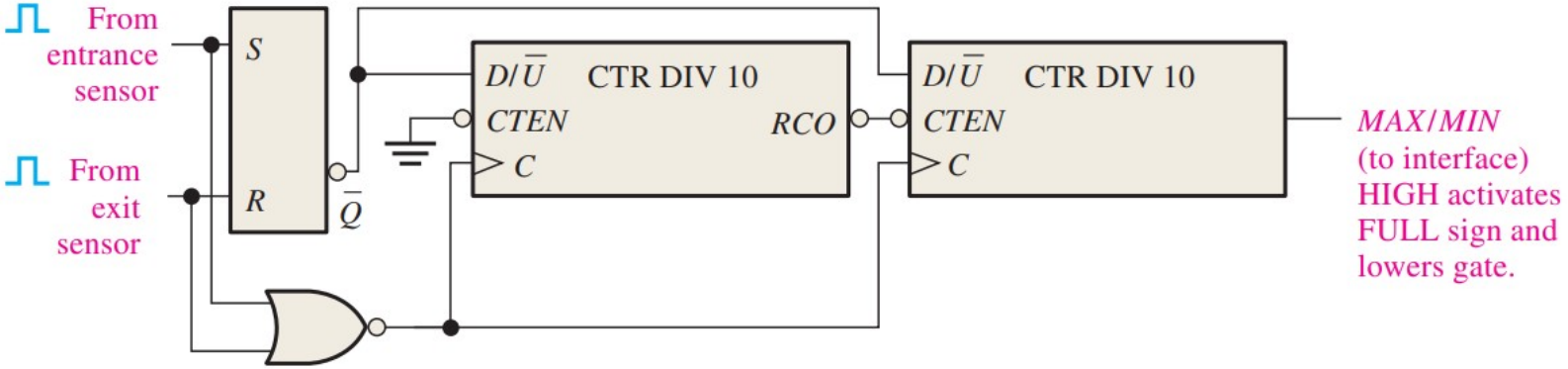
- Digital Clock
- Car Parking Spot Indicator
- Serial to Parallel Conversion

Digital Clock

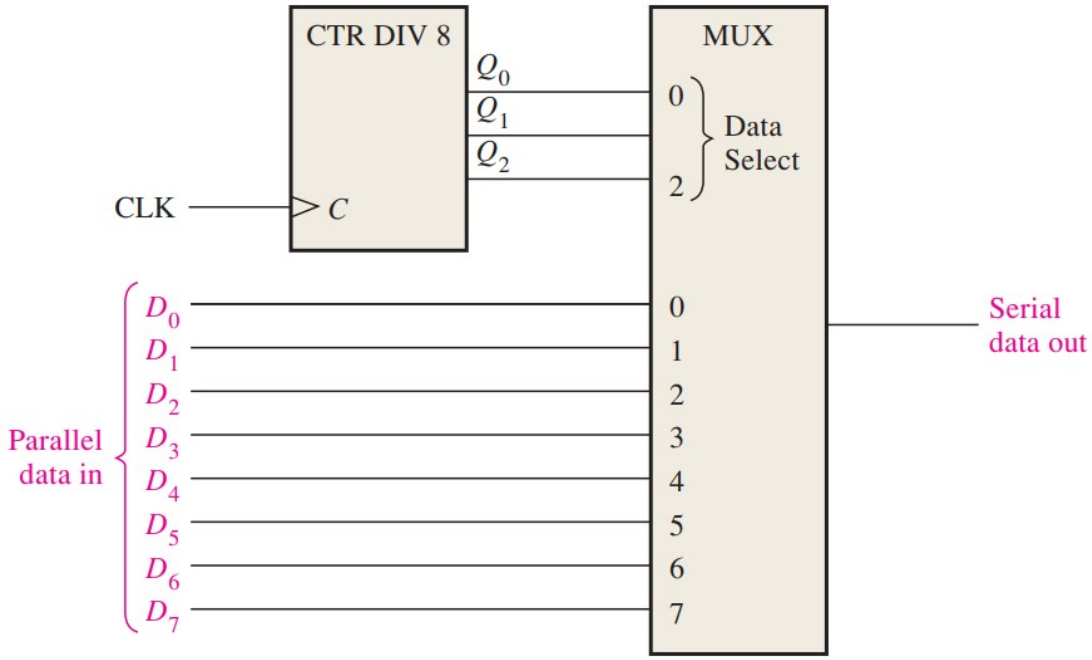


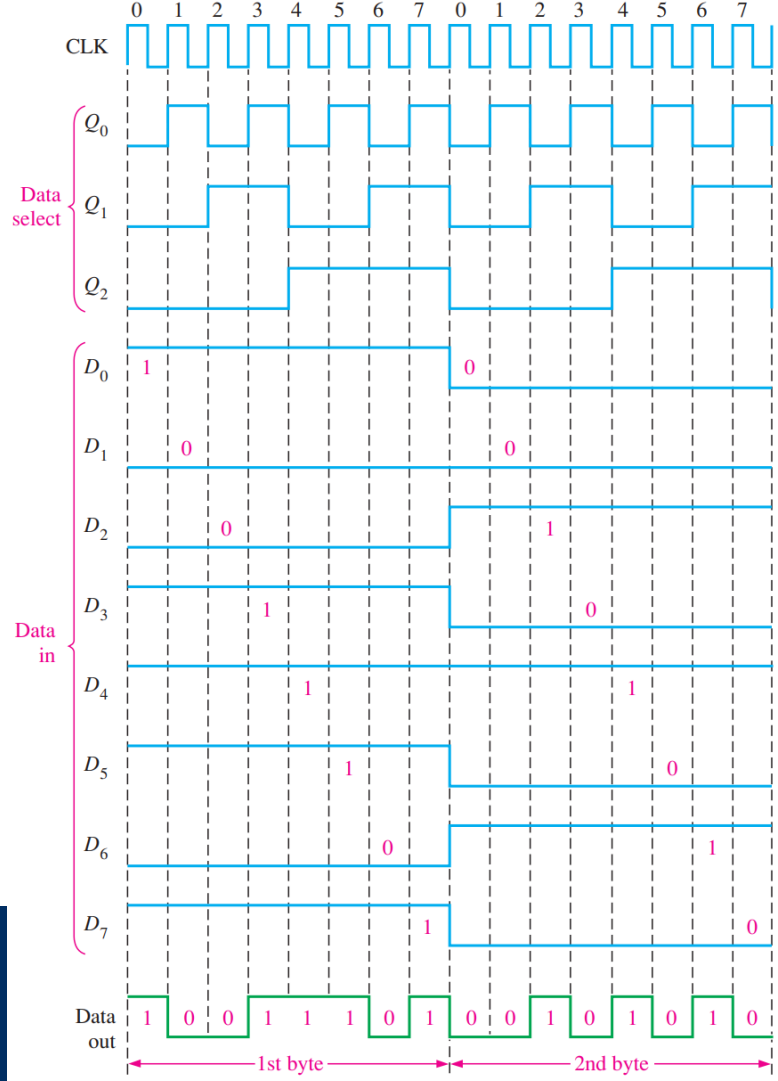
Car Parking Spot Indicator



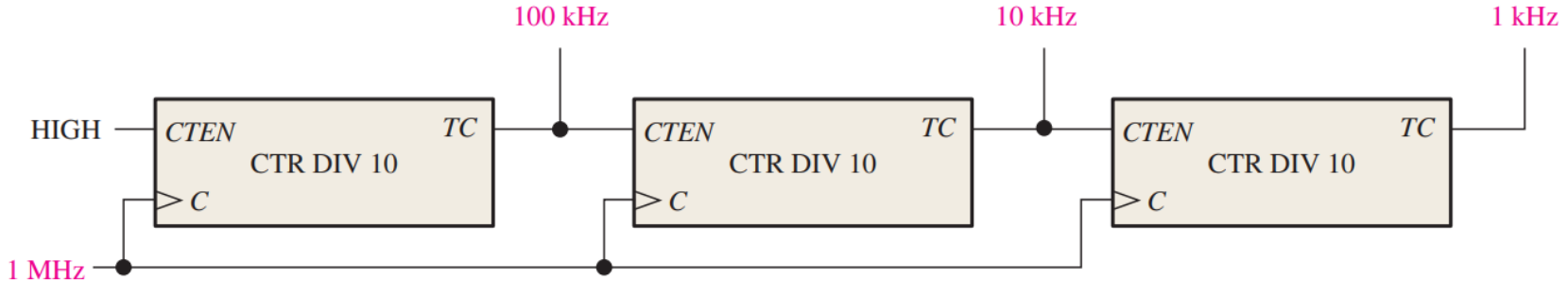


Parallel to Serial

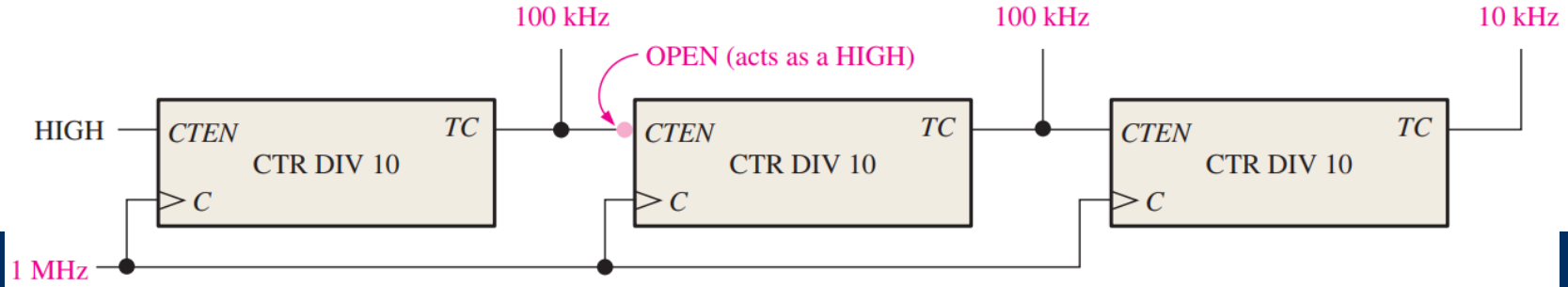




Troubleshooting



Normal operation



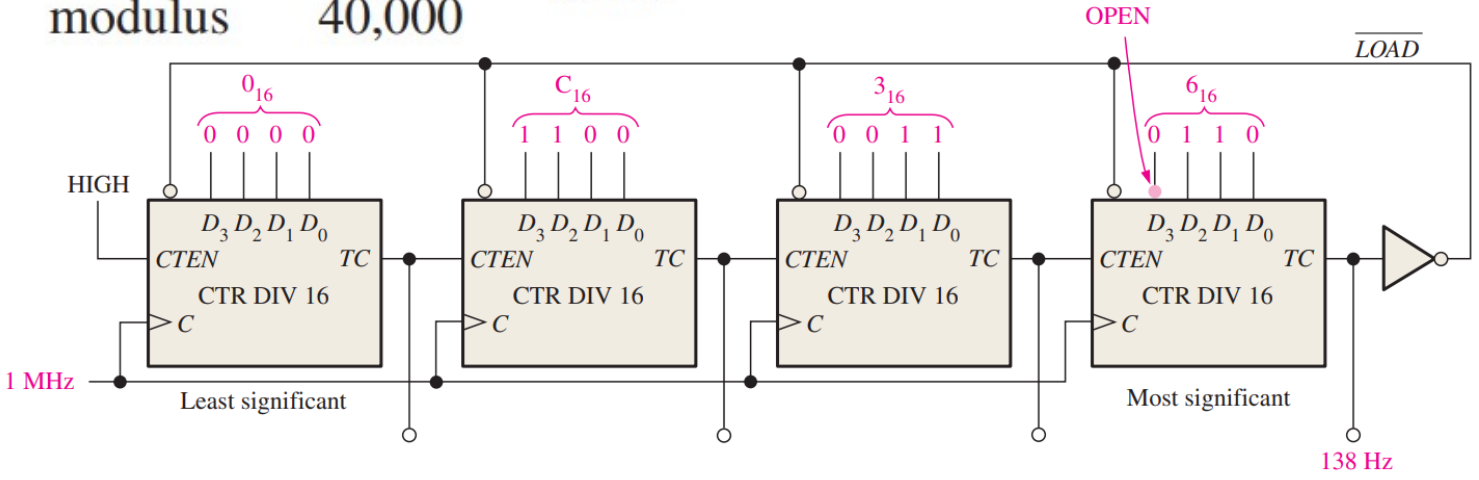
Count Enable (*CTEN*) input of second counter open

Troubleshooting

$$f_{out} = \frac{f_{in}}{\text{modulus}} = \frac{1\text{ MHz}}{7232} \cong 138\text{ Hz}$$

- Open can change the output frequency
  - In this chip, open acts like a high input

$$f_{out} = \frac{f_{in}}{\text{modulus}} = \frac{1\text{ MHz}}{40{,}000} = 25\text{ Hz}$$



Reading

- This lecture
  - Sections 9.6-9.10
- Next lecture
  - 9.5, Ch7 and Ch8 Applied Logic