CPE201
Digital Design

By Benjamin Haas

Class 12: Combinational Logic

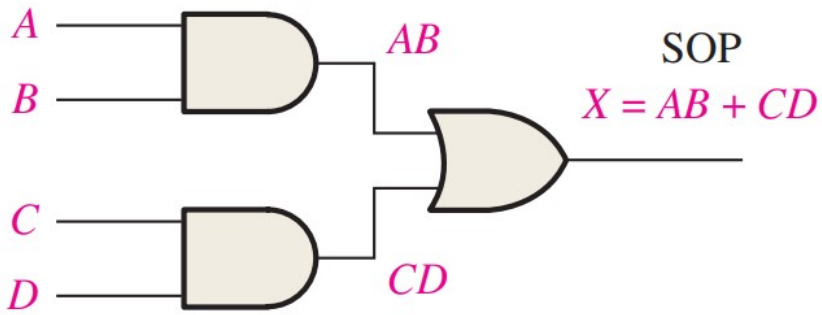
University of Nevada, Reno

Focus on Implementation

- Creating circuits from logic in Ch4
  - AND-OR Logic
  - AND-OR-Invert Logic
- Quick Review
  - XOR
  - XNOR

AND-OR Logic

- What you already know from SOP expressions
- Example: AB + CD

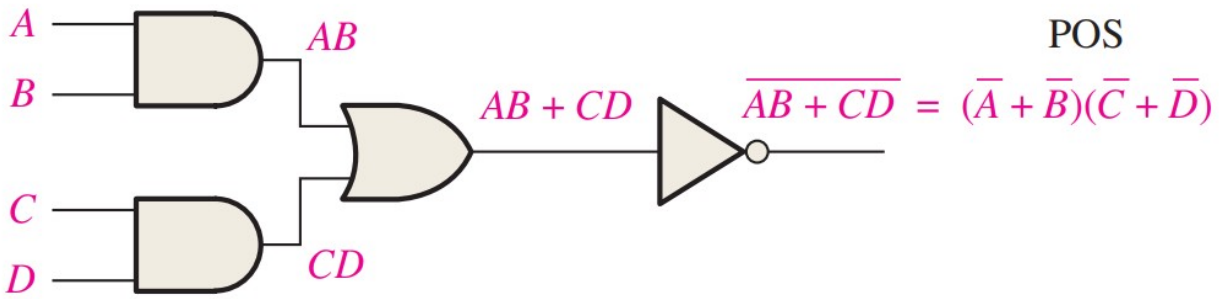


AND-OR-Invert Logic

- Implements POS expressions
  - Heavy use of DeMorgan's
  - Implementation looks like SOP

Example

- (A′ + B′)(C′ + D′) = (AB)′(CD)′ = ((AB)′(CD)′)″
  - Two NOTs would cancel, distribute one
- =(AB + CD)′



Example

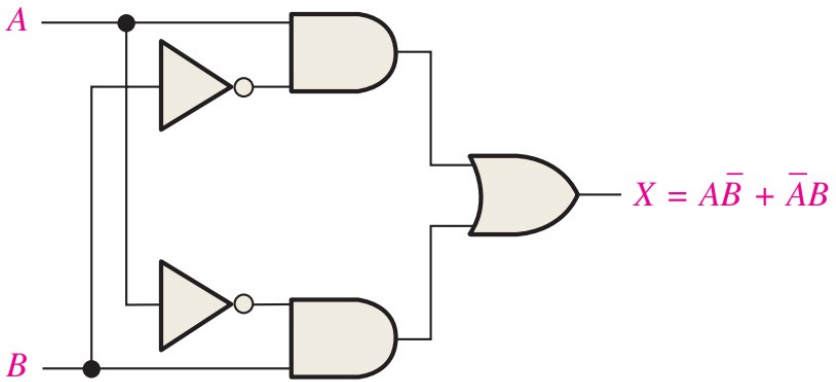
- Convert POS terms to Invert SOP terms

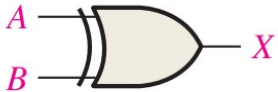
- (A + B’ + C’)(A’ + B’ + C)(A’ + B + C)=
- (A’BC + ABC’ + AB’C’)’

XOR

- Simplify your logic

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

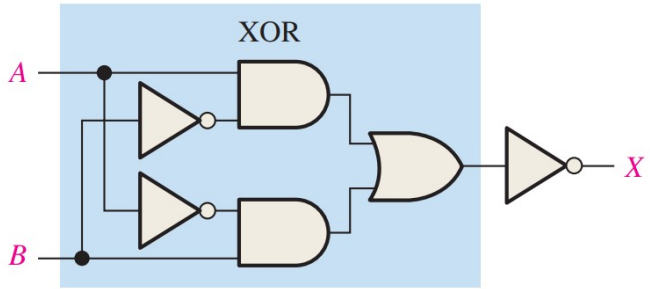




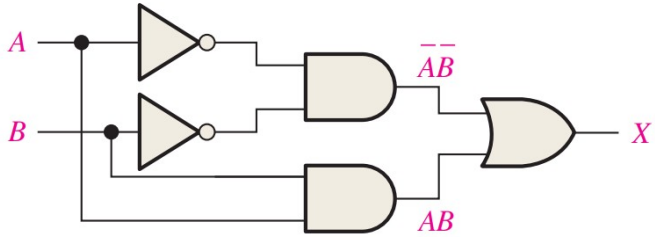
XNOR

- Simplify your logic

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1



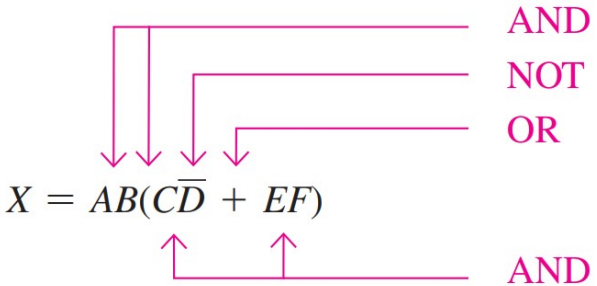
(a) $X = A\overline{B} + \overline{A}B$



(b) $X = \overline{A}\overline{B} + AB$

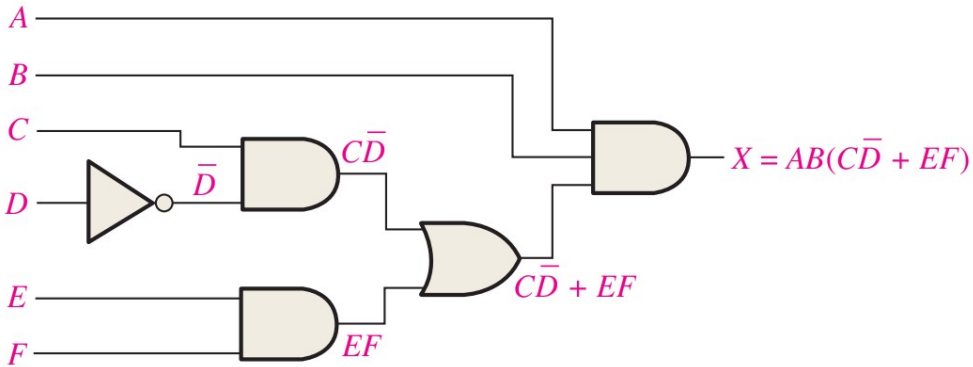
Implementation

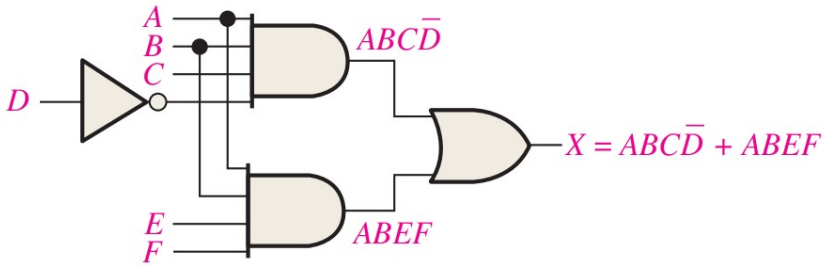
- Order of operations for Boolean expressions
  - Same as regular math expression symbols



Example

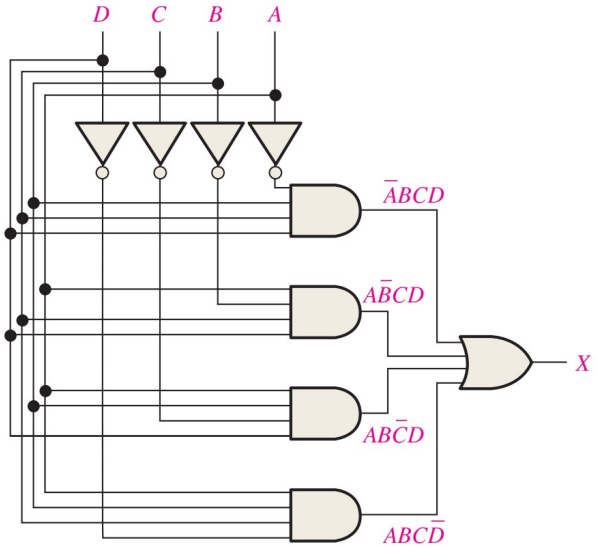
- AB(CD’ + EF) = ABCD’ + ABEF
  - Distributed to SOP



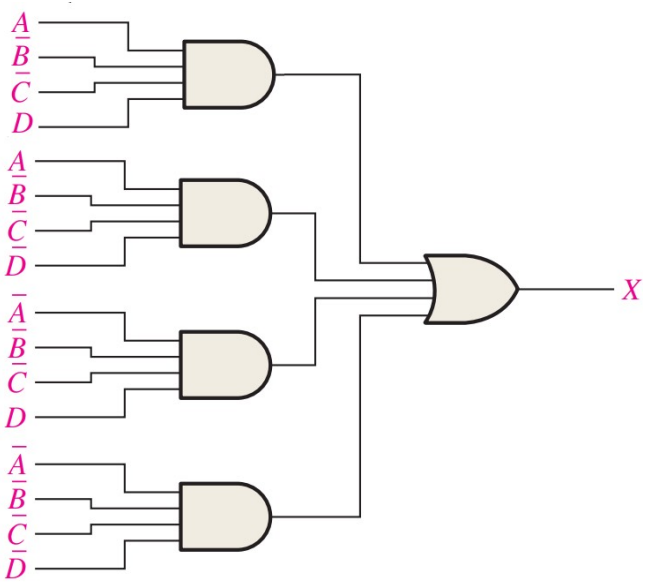


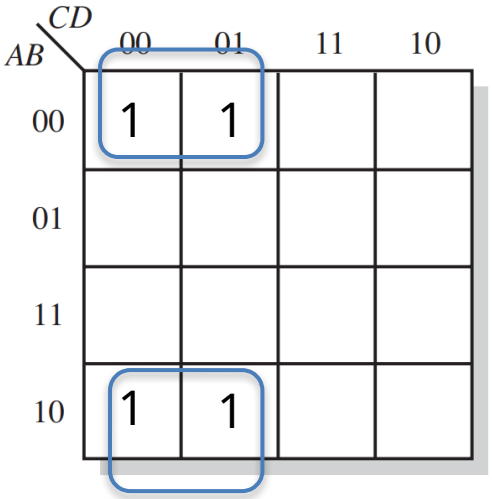
Ye Olde Grid

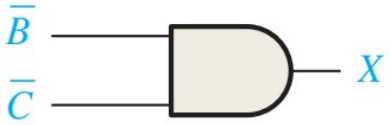
- Makes Standard SOP
  - Add a NOT and get Standard



Minimize


$\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$
$\overline{A}\,\overline{B}\,\overline{C}\,D$
$\overline{A}\,B\,\overline{C}\,\overline{D}$
$\overline{A}\,B\,\overline{C}\,D$
X


CD
AB
00
01
11
10
1
1
1
1


$\overline{B}$
$\overline{C}$
X

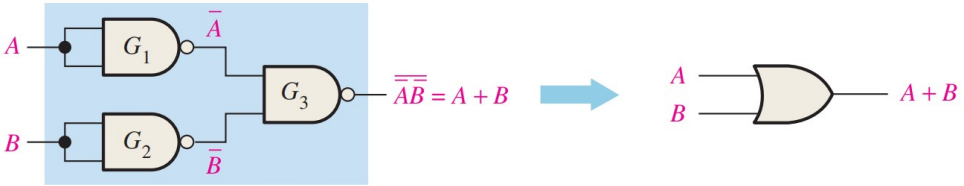
Universal Gates

- NAND and NOR
  - You can make every other gate with them
- AND and OR are not universal
  - Can’t make NOT

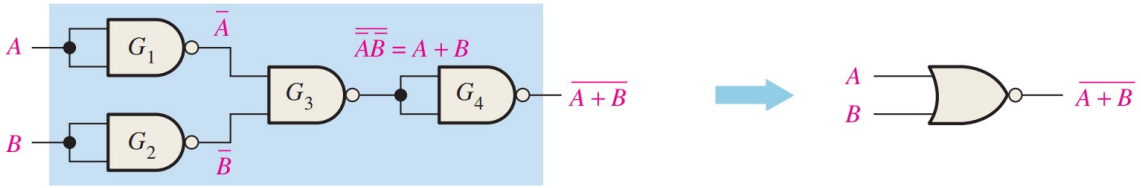
NAND to Other Gates

(a) One NAND gate used as an inverter

(b) Two NAND gates used as an AND gate



(c) Three NAND gates used as an OR gate

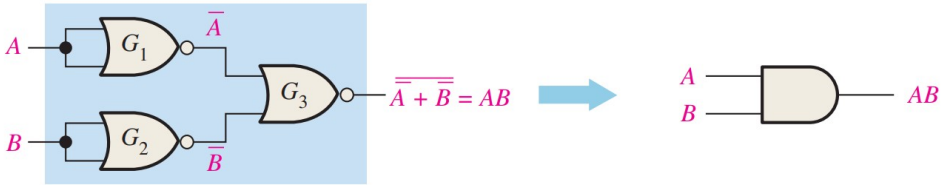


(d) Four NAND gates used as a NOR gate

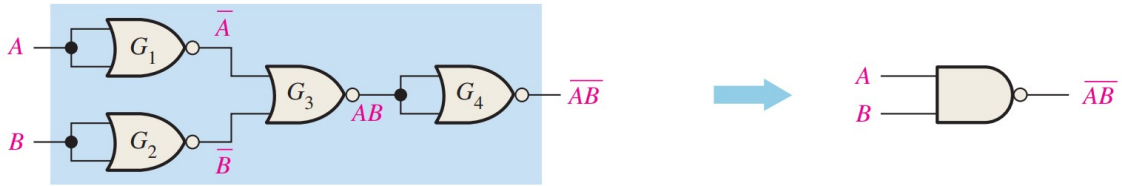
NOR to Other Gates

(a) One NOR gate used as an inverter

(b) Two NOR gates used as an OR gate



(c) Three NOR gates used as an AND gate



(d) Four NOR gates used as a NAND gate

Reading

- This lecture
  - Sections 5.1-5.3
- Next lecture
  - Sections 5.4-5.5, 3.8