

CPE201

Digital Design

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Class 14: Adders



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Outline

- Half Adder
- Full Adder
- Parallel Adders
- Ripple vs Look Ahead Carry



Combinational Logic Applications

- You now know the basics
 - Let's make cool stuff!
 - Adders
 - Comparators
 - Decoders/Encoders
 - Mux/Demux
 - And more!



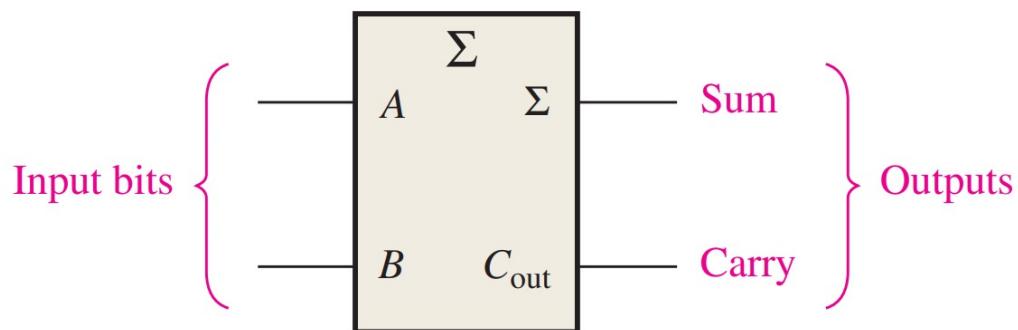
Half Adder

- Recall binary addition
 - $0 + 0 = 0$
 - $0 + 1 = 1$
 - $1 + 0 = 1$
 - $1 + 1 = 10$
- A circuit that does this is a half adder



Half Adder

- 2 inputs, 2 outputs
 - Addition of 2 bits



A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = sum

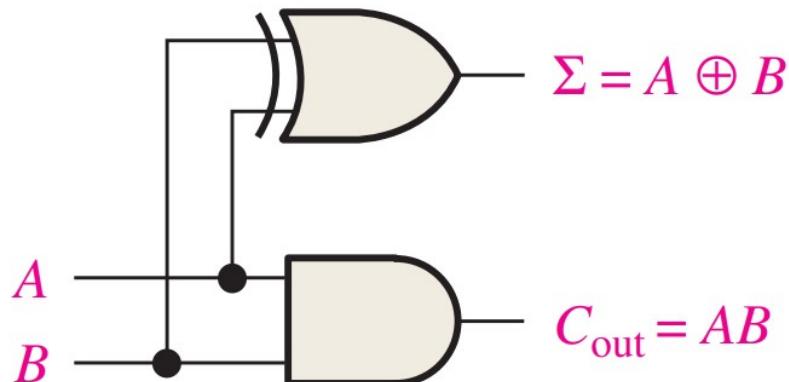
C_{out} = output carry

A and B = input variables (operands)



Half Adder

- $C_{\text{out}} = AB$
- $\Sigma = A \oplus B$



A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = sum

C_{out} = output carry

A and B = input variables (operands)



Half Adder+

- Can add two input bits together
 - Not complete for full binary addition

In this case, the carry bit from second column becomes a sum bit.

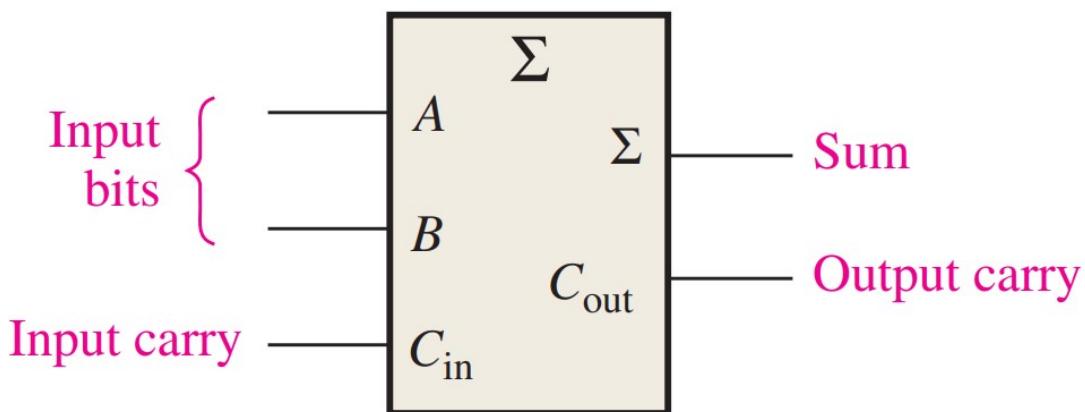
$$\begin{array}{r} & \text{Carry bit from right column} \\ & \downarrow \\ 1 & \\ 11 & \\ + 01 & \\ \hline 100 & \uparrow \end{array}$$

- Needs input carry AND output carry



Full Adder

- 3 inputs, 2 outputs
 - Addition of 3 bits



A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{in} = input carry, sometimes designated as CI

C_{out} = output carry, sometimes designated as CO

Σ = sum

A and B = input variables (operands)



Full Adder

- $C_{\text{out}} = AB + (A \oplus B)C_{\text{in}}$
- $\Sigma = (A \oplus B) + C_{\text{in}}$
- Not as obvious

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{in} = input carry, sometimes designated as CI

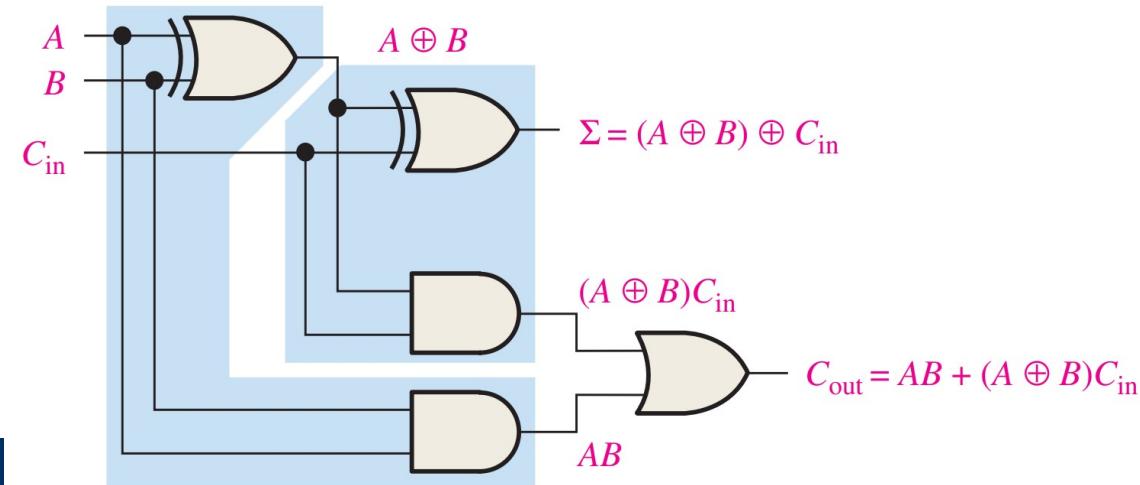
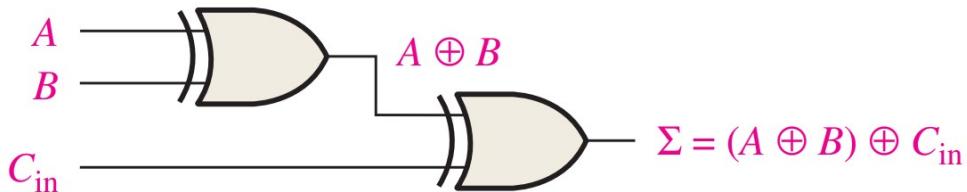
C_{out} = output carry, sometimes designated as CO

Σ = sum

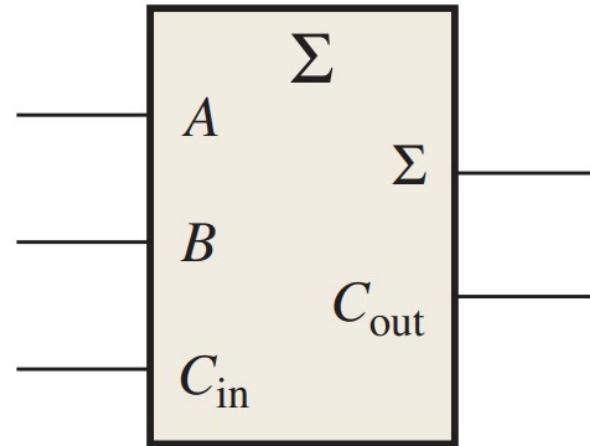
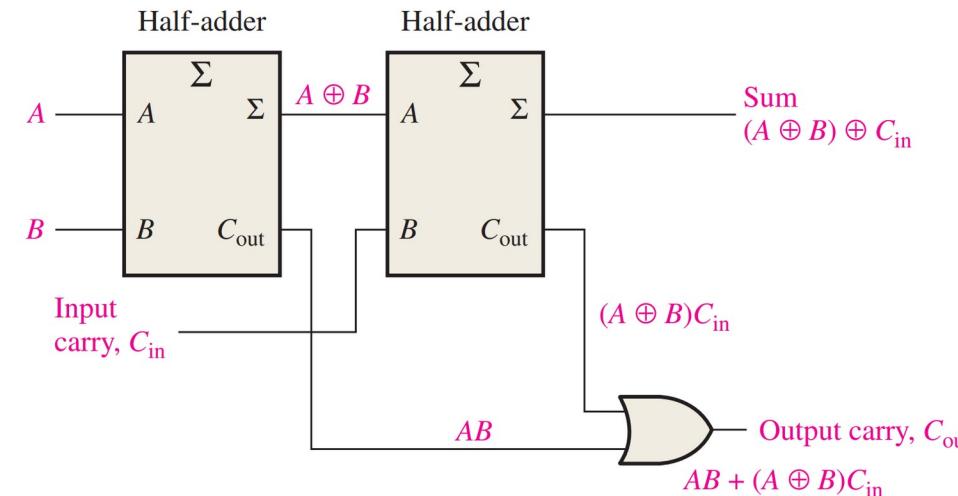
A and B = input variables (operands)



Full Adder



Full Adder



Full Adder+

- Can add three input bits together
 - Complete for full binary addition
 - Let's do that!

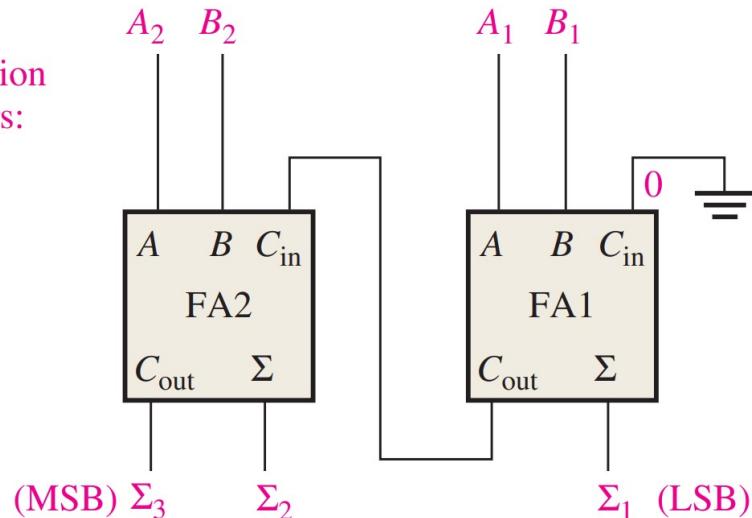


Parallel Binary Adders

- Two or more full adders cascaded

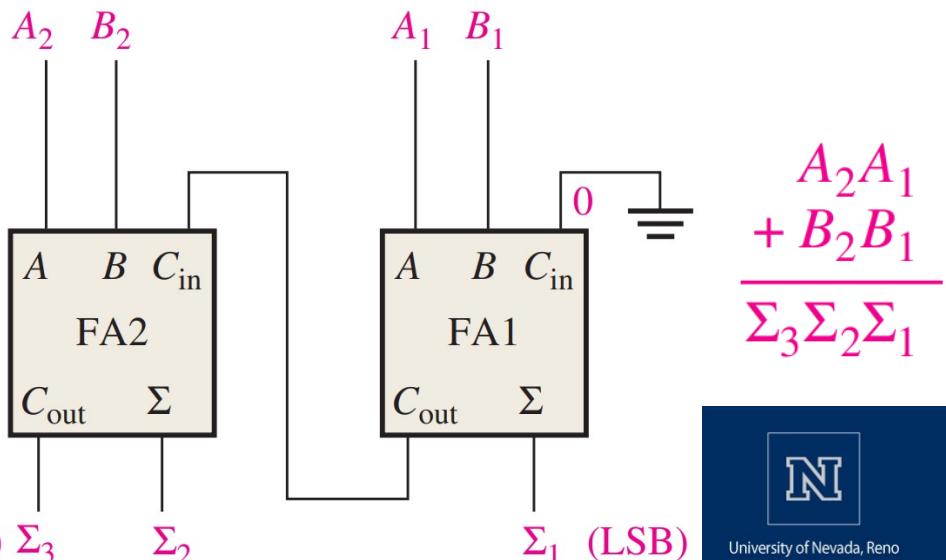
General format, addition
of two 2-bit numbers:

$$\begin{array}{r} A_2 A_1 \\ + B_2 B_1 \\ \hline \Sigma_3 \Sigma_2 \Sigma_1 \end{array}$$



Example

- For $11 + 01 = 100$
- $A_1=1$ $A_2=1$ $B_1=1$ $B_2=0$



A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{in} = input carry, sometimes designated as CI

C_{out} = output carry, sometimes designated as CO

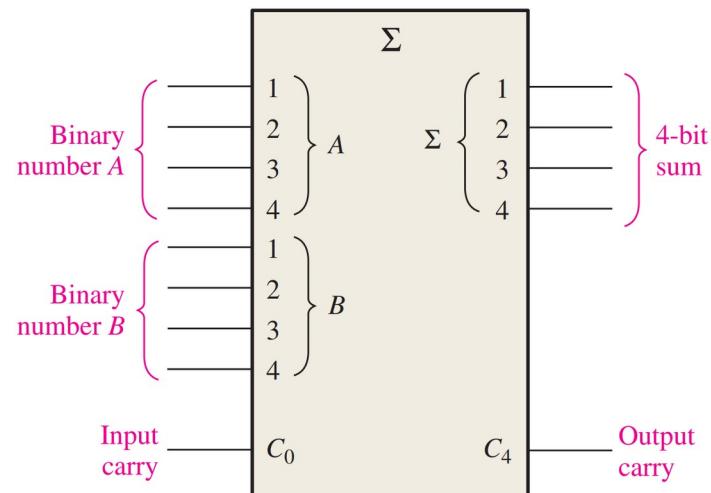
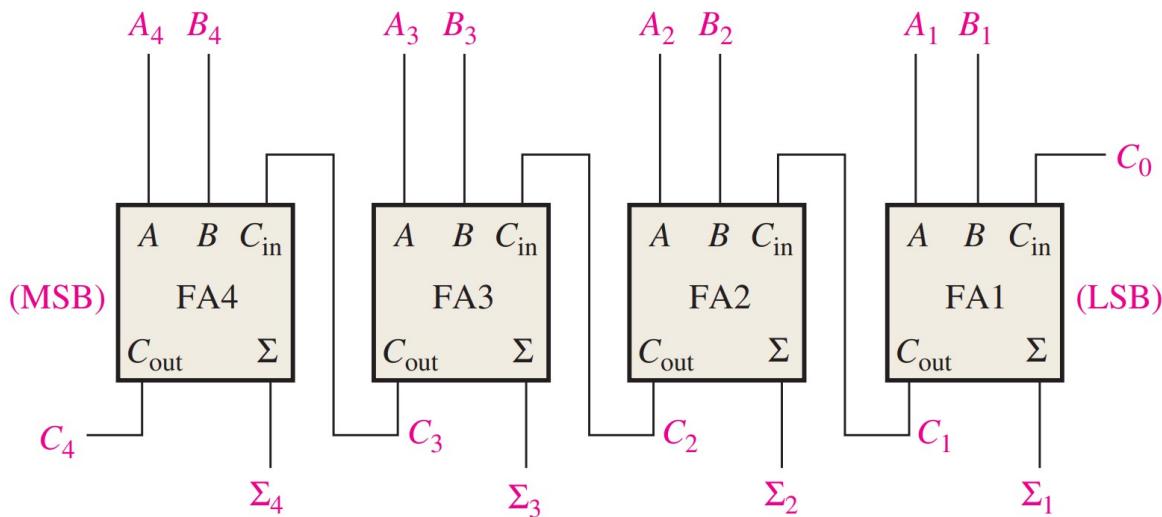
Σ = sum

A and B = input variables (operands)

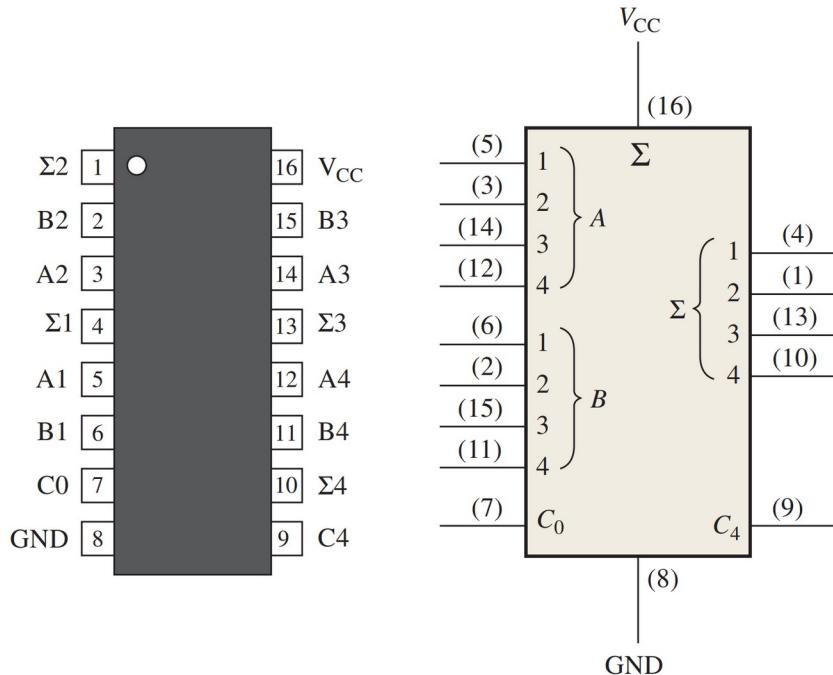


4-Bit Parallel Adder

- You can buy those (74xx283)



Nibble Adder

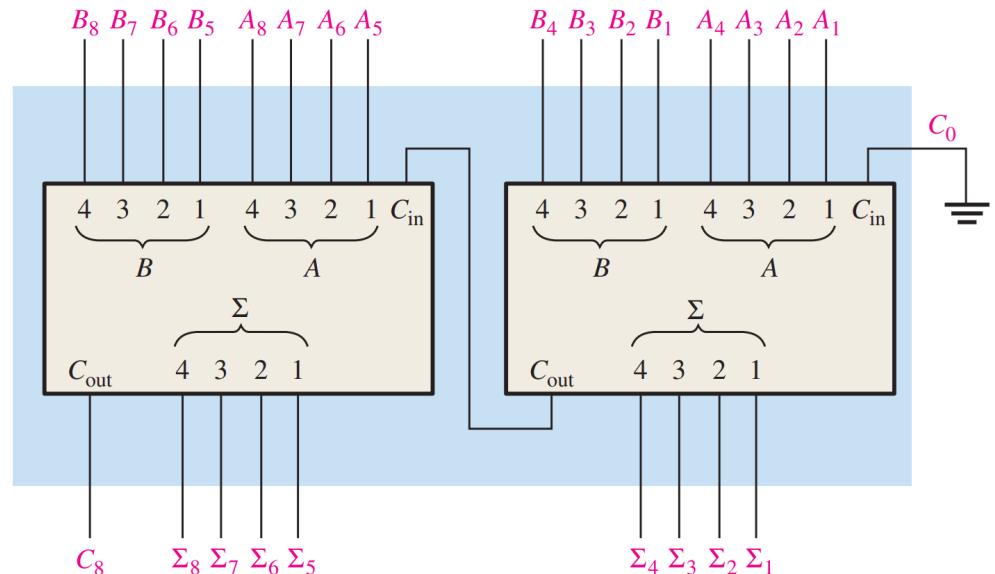


C_{n-1}	A_n	B_n	Σ_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



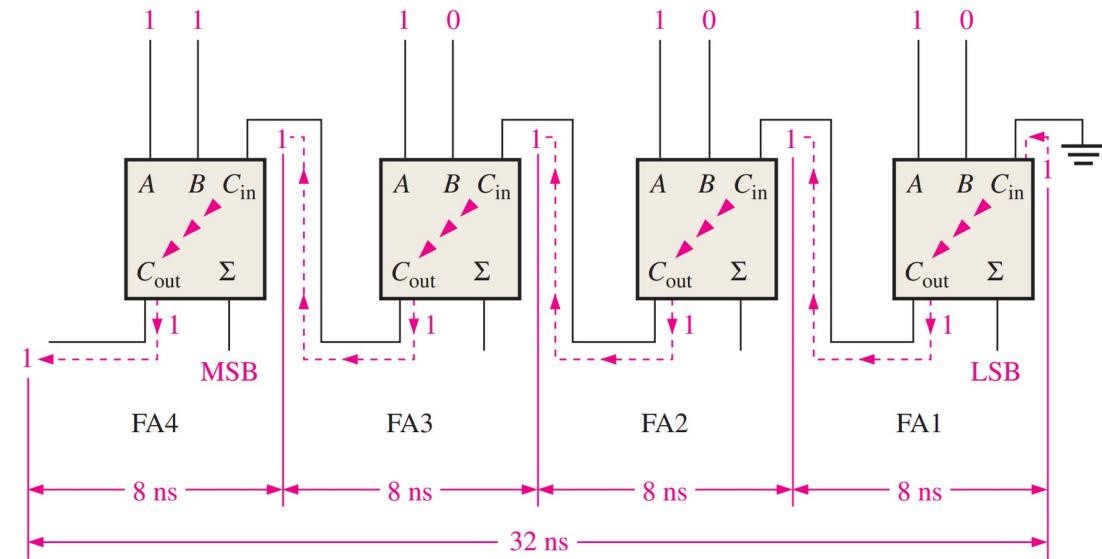
Byte Adder

- More Cascading



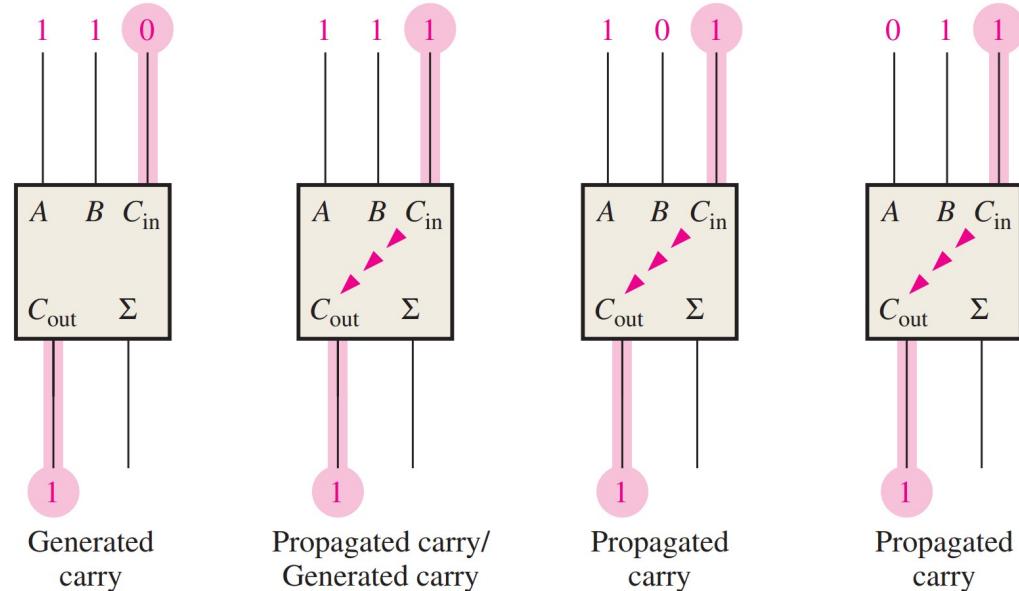
Problem = Ripple Carry Adder

- Carry bits are slow
- Total time = $(3n)\tau$ (time for 1 bit of adding)
- Mult/Division =
Add/Subtr
- Faster addition
makes all others
faster



Generated and Propagated Carry

- $C_g = AB$
- $C_p = A + B$ book
- $C_p = A \cdot B$ web
- $\Sigma = C_p \cdot C_{in}$
- $C_{out} = C_g + C_p \cdot C_{in}$
- $C_{out} = AB + (A \cdot B)C_{in}$ (Full Adder)



Carry Look-Ahead Adder

- All inputs are available at the same time
 - Create all C_g s and C_p s at the same time
- $C_{g,i} = A_i B_i$
- $C_{p,i} = A_i \oplus B_i$
- Same as a Half Adder
- $i = 0 \dots 3$

- Half Adder:
 - $C_{out} = AB$
 - $\Sigma = A \oplus B$



Carry Look-Ahead Adder

- Create all Carry bits
- $C_{(i+1)} = C_{g,i} + C_{p,i} C_i$
- $C_0 = C_{in}$
- $C_4 = C_{out}$



Carry Look-Ahead Adder

- Last, create all sum bits
- $\Sigma_i = C_{p,i} C_i$



Carry Look-Ahead Adder

- Half Adder:
- $C_{out} = AB$
- $\Sigma = A \oplus B$



Carry Look-Ahead Adder

- 3 Stages of Logic with no ripple
- Total time = 4τ (time for 1 bit of adding)
- Ripple carry takes 9τ for 4 bits
- Tradeoff of more complex circuitry (w/ more gates)



Reading

- This lecture
 - Sections 6.1-6.3
- Next lecture
 - Sections 6.4-6.6

