# CPE201
# Digital Design

By Benjamin Haas

## Class 23: State Machines and Counters

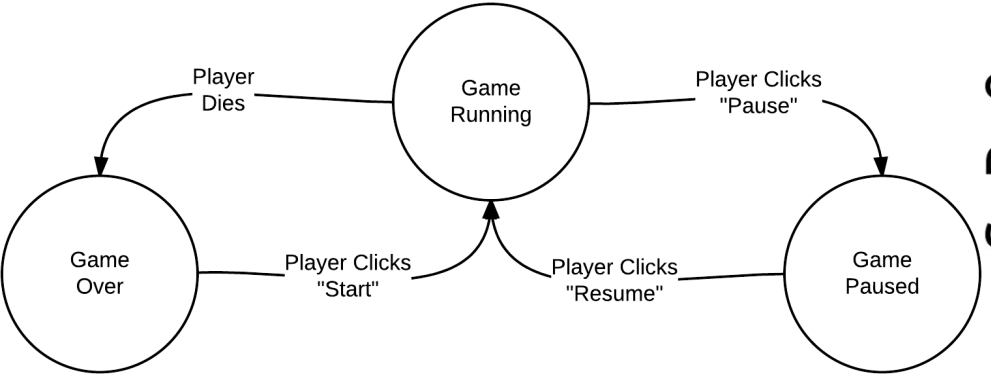
University of Nevada, Reno

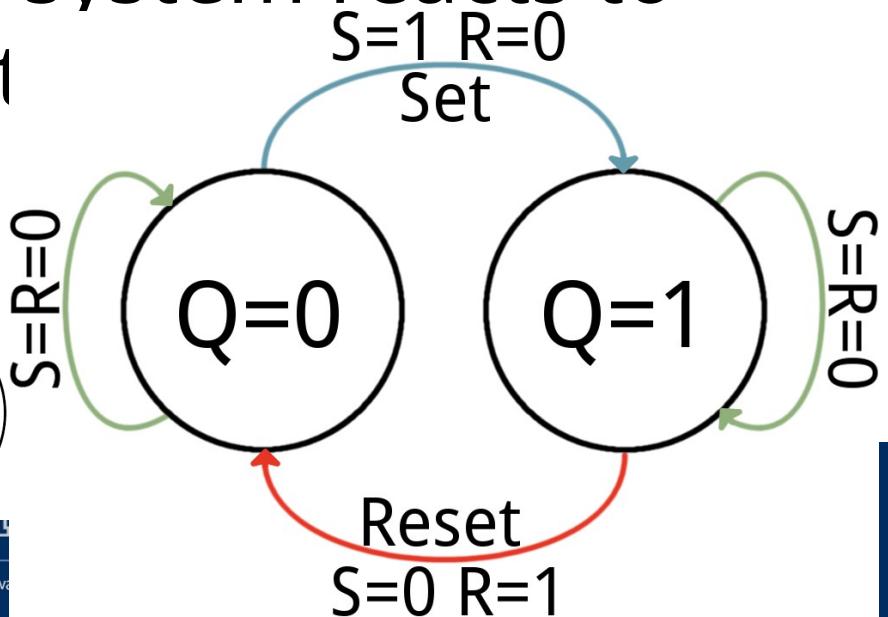
# Outline

- Finite State Machines
  - Moore
  - Mealy
- Asynchronous Counters
- Synchronous Counters
- Bidirectional Counters

# Finite State Machines

- Not infinite
- Describes how your system reacts to inputs and gives out



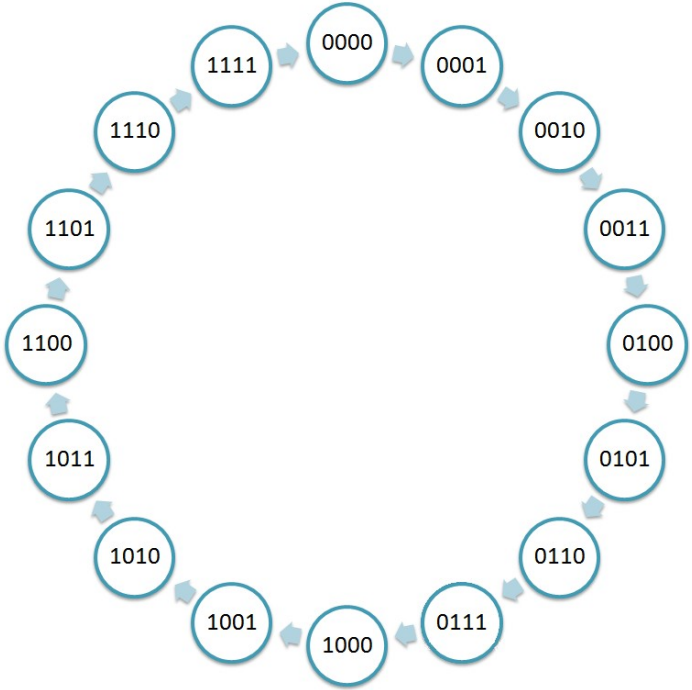



# State Machines

- Moore – Output depends on machine state
  - Simpler design, requires more states and circuitry
- Mealy – Output depends on machine state and inputs
  - Complex design, less states and circuitry

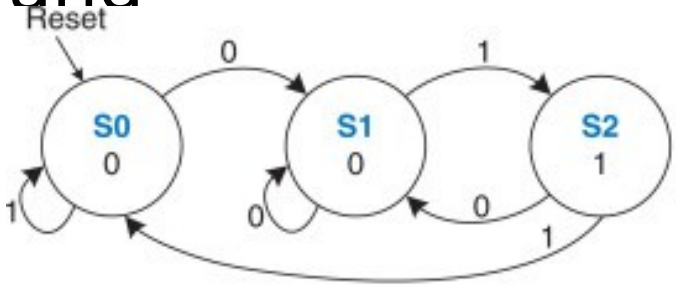
# State Machines

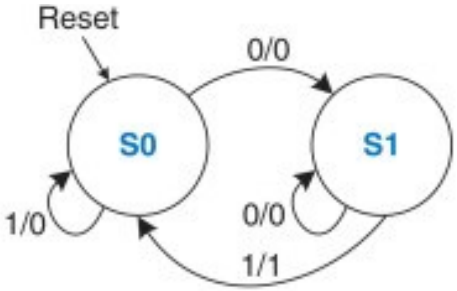
- Counters are simple
  - Moore machines
  - No inputs



# Sequence Detection

- Typical example, but extensible
  - Detects sequence of 01, outputs 1 when found



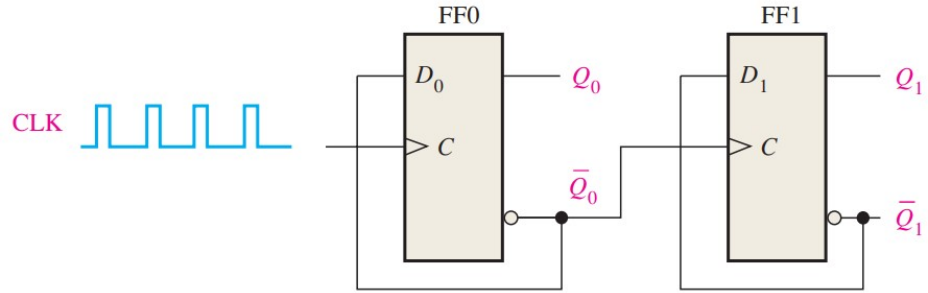



# Vocab

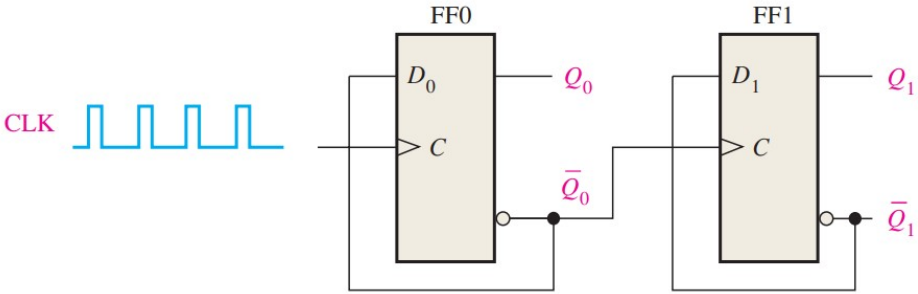
- Synchronous – events happen with a fixed time relationship
  - In counters, CLK goes to all flip-flops
- Asynchronous – no fixed time relationship
  - In counters, CLK does not go to all flip-flops

# Asynchronous Binary Counters

- 2-bits, so $2^2$ counts
- LSB = FF0
- C is positive edge triggered
- CLK only goes into FF0, FF1 is fed by $Q_0$’
- Ripple causes it to be asynchronous



# Asynchronous Binary Counters

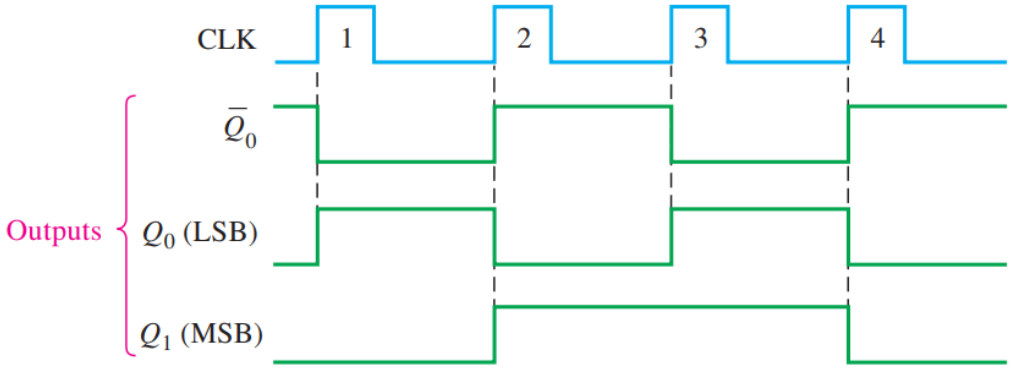



| Clock Pulse | $Q_1$ | $Q_0$ |
|---|---|---|
| Initially | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |
| 4 (recycles) | 0 | 0 |

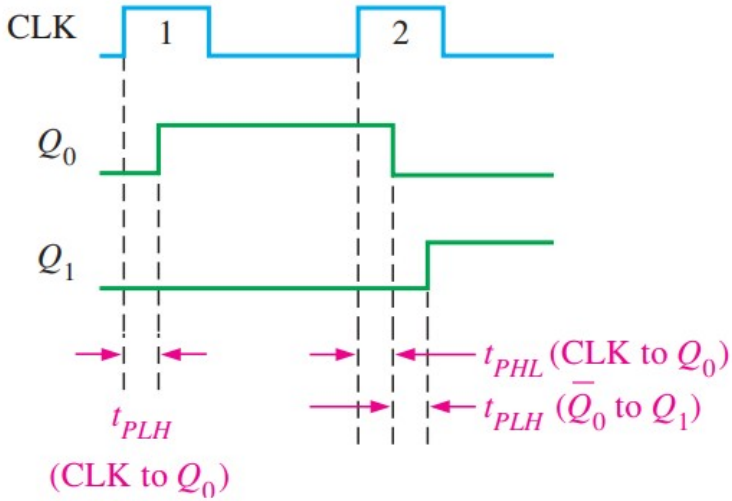
- Outputs read in binary 0…3

# Asynchronous Binary Counters

## Ideal

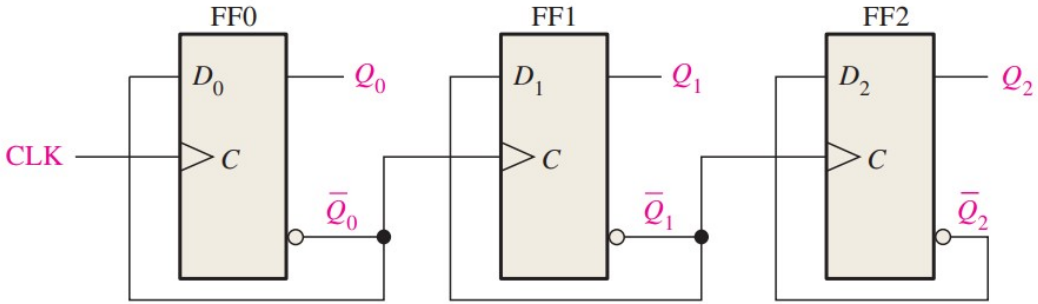



## Real



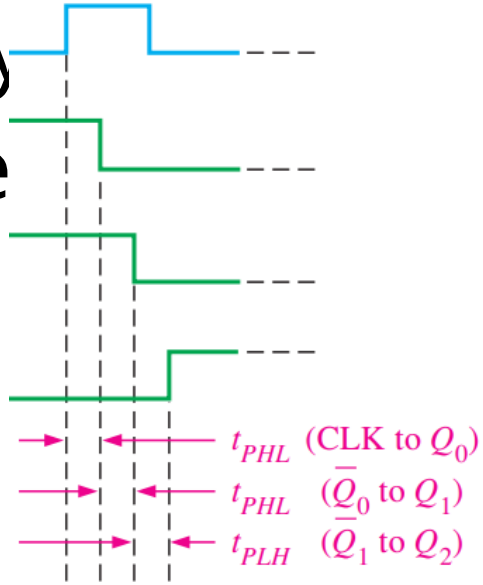
# Ripple Binary Counter

- Other name for Asynchronous Counter
- 3 bits, so $2^3$ states, counts 0..7
- Exactly matches counting app from FFs
- Just add FFs

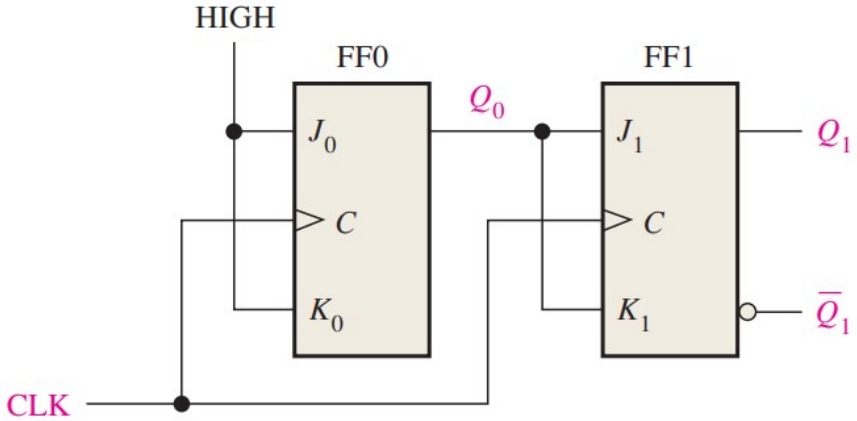


# Problem

- A large counter = many delay
- If ripple not complete before next CLK
  - The circuit can desynchronize



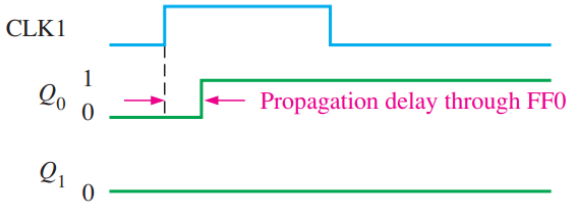
# Synchronous Binary Counter

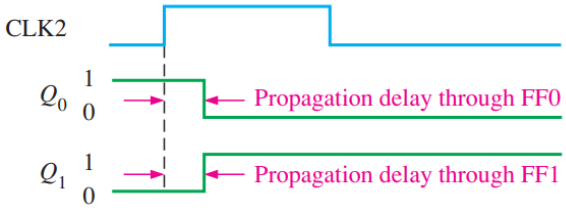


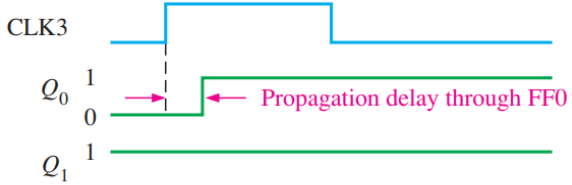

Truth table for a positive edge-triggered J-K flip-flop.

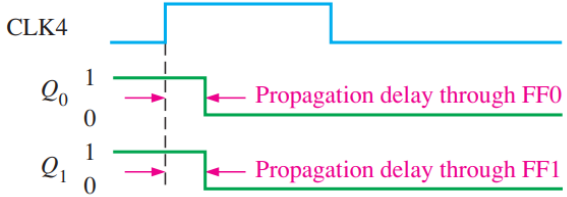
| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| $J$ | $K$ | CLK | $Q$ | $\overline{Q}$ | Comments |
| 0 | 0 | ↑ | $Q_0$ | $\overline{Q}_0$ | No change |
| 0 | 1 | ↑ | 0 | 1 | RESET |
| 1 | 0 | ↑ | 1 | 0 | SET |
| 1 | 1 | ↑ | $\overline{Q}_0$ | $Q_0$ | Toggle |

↑ = clock transition LOW to HIGH
$Q_0$ = output level prior to clock transition



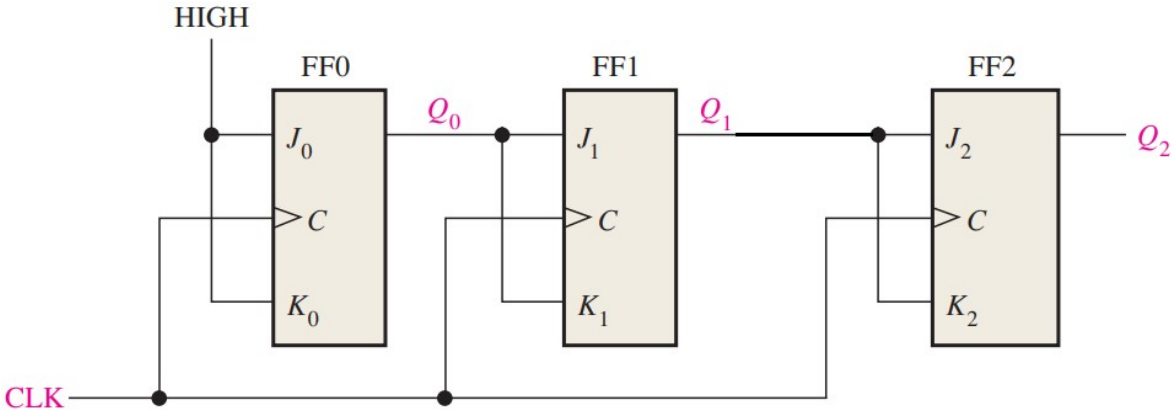



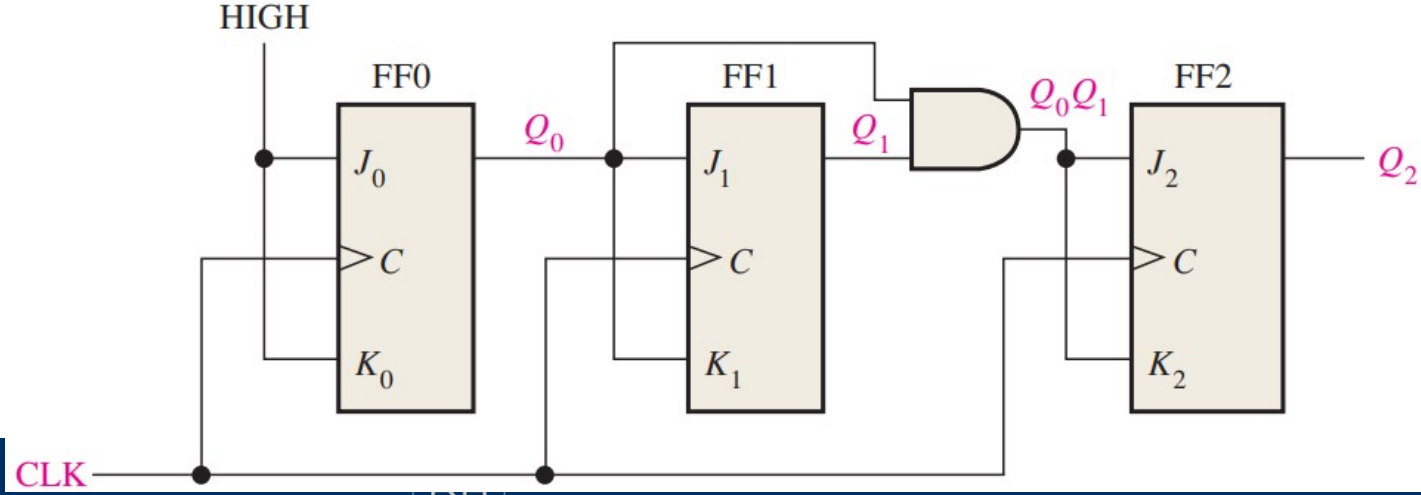
# Synchronous Binary Counter

- Can’t just add for JK FFs
  - 0, 1, 2, 7, 0, …

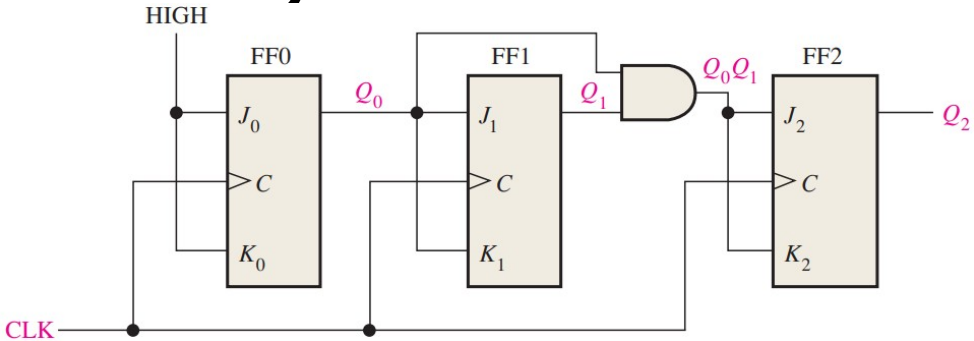


# Synchronous Binary Counter

- AND only lets Q2 toggle when Q1 and Q0 are 1, like in counting

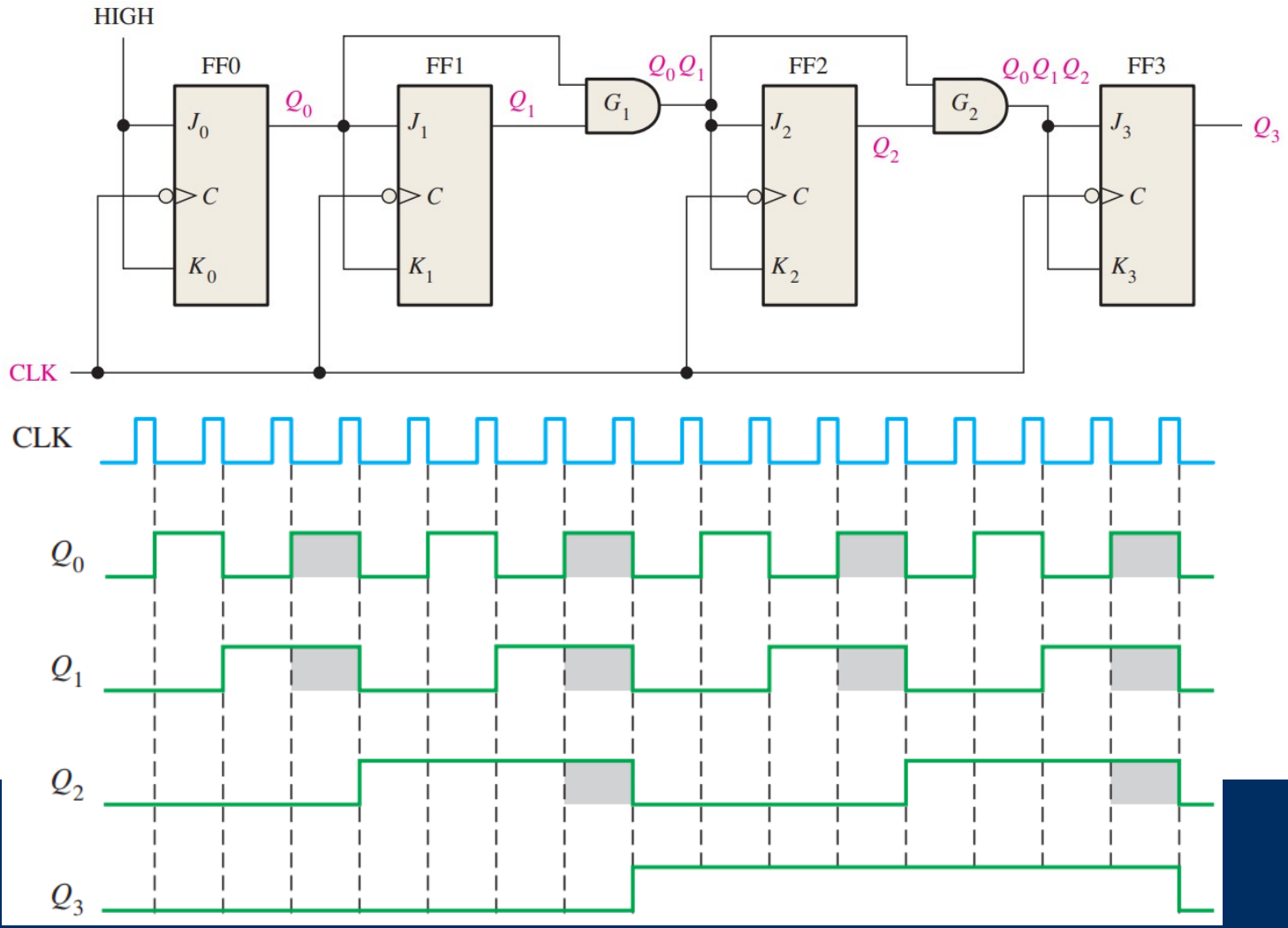


# Synchronous Binary Counter



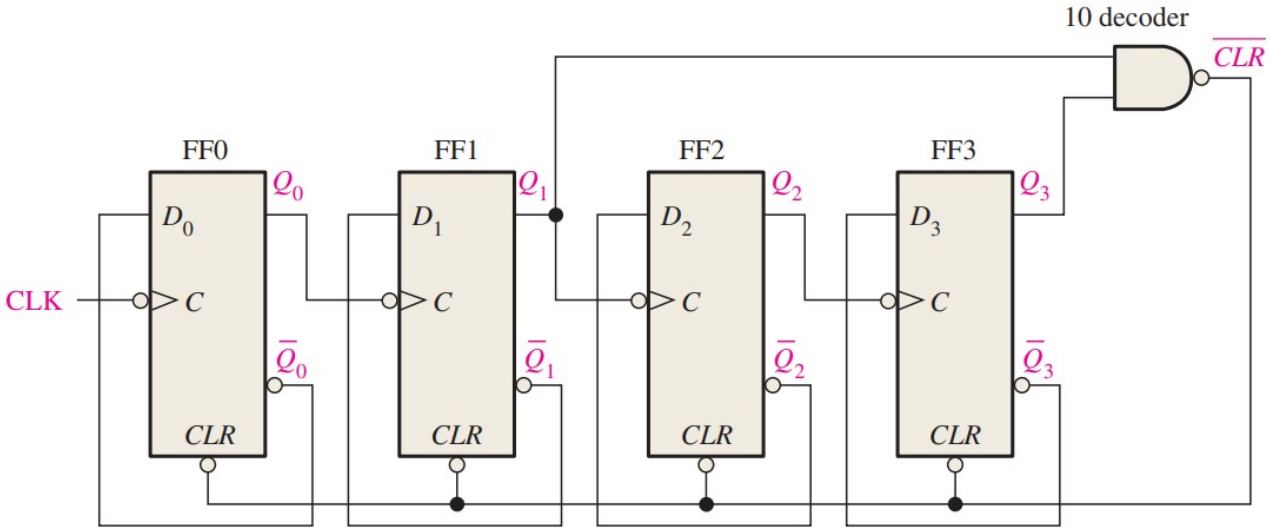

| Clock Pulse | Outputs $Q_2$ | $Q_1$ | $Q_0$ | J-K Inputs $J_2$ | $K_2$ | $J_1$ | $K_1$ | $J_0$ | $K_0$ | At the Next Clock Pulse FF2 | FF1 | FF0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Initially | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | NC* | NC | Toggle |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | NC | Toggle | Toggle |
| 2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | NC | NC | Toggle |
| 3 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Toggle | Toggle | Toggle |
| 4 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | NC | NC | Toggle |
| 5 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | NC | Toggle | Toggle |
| 6 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | NC | NC | Toggle |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Toggle | Toggle | Toggle |
| | | | | | | | | | | Counter recycles back to 000. | | |

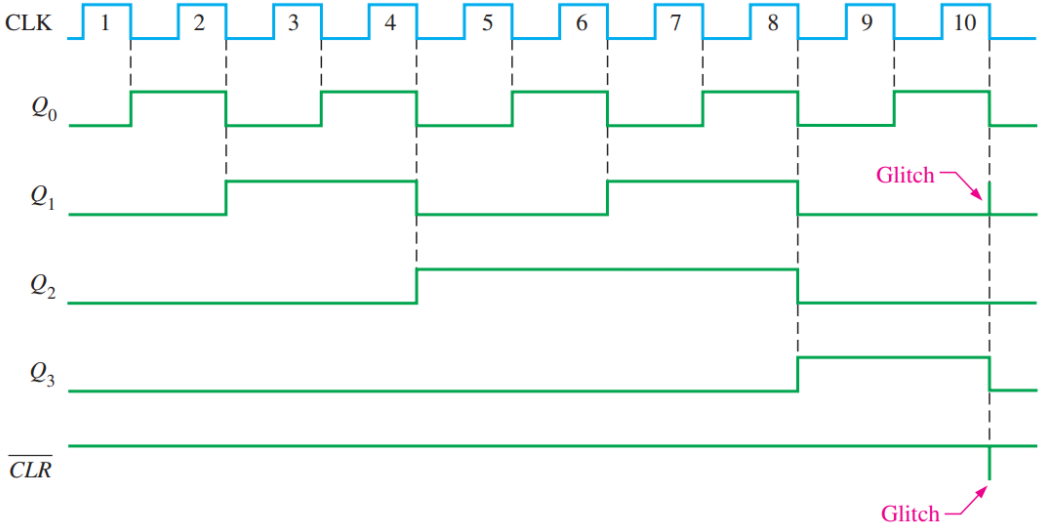
*NC indicates *No Change*.


HIGH
FF0
FF1
FF2
FF3
$J_0$
$C$
$K_0$
$Q_0$
$J_1$
$C$
$K_1$
$Q_1$
$G_1$
$Q_0Q_1$
$J_2$
$C$
$K_2$
$Q_2$
$G_2$
$Q_0Q_1Q_2$
$J_3$
$C$
$K_3$
$Q_3$
CLK
CLK
$Q_0$
$Q_1$
$Q_2$
$Q_3$

# Truncated Asynchronous Counter

- Usually $2^n$ states, with n flip-flops
- Reset the counter early, truncate the count
- Create other counts
- There are synch and asynch versions
- Next is MOD10 asynch (counts 0 to 9)


10 decoder
$\overline{CLR}$
FF0
FF1
FF2
FF3
$Q_0$
$Q_1$
$Q_2$
$Q_3$
$D_0$
$D_1$
$D_2$
$D_3$
CLK
C
$\overline{Q}_0$
$\overline{Q}_1$
$\overline{Q}_2$
$\overline{Q}_3$
CLR


CLK
1
2
3
4
5
6
7
8
9
10
$Q_0$
$Q_1$
$Q_2$
$Q_3$
$\overline{CLR}$
Glitch
Glitch

# Bidirectional Counter

- Also an up/down coun
- Counts in either direct

UP UP

0, 1, 2, 3, 4, 5, 4, 3, 2, 3, 4, 5, 6, 7, 6, 5, etc.

DOWN DOWN

| Clock Pulse | Up | $Q_2$ | $Q_1$ | $Q_0$ | Down |
|---|---|---|---|---|---|
| 0 | | 0 | 0 | 0 | |
| 1 | | 0 | 0 | 1 | |
| 2 | | 0 | 1 | 0 | |
| 3 | | 0 | 1 | 1 | |
| 4 | | 1 | 0 | 0 | |
| 5 | | 1 | 0 | 1 | |
| 6 | | 1 | 1 | 0 | |
| 7 | | 1 | 1 | 1 | |

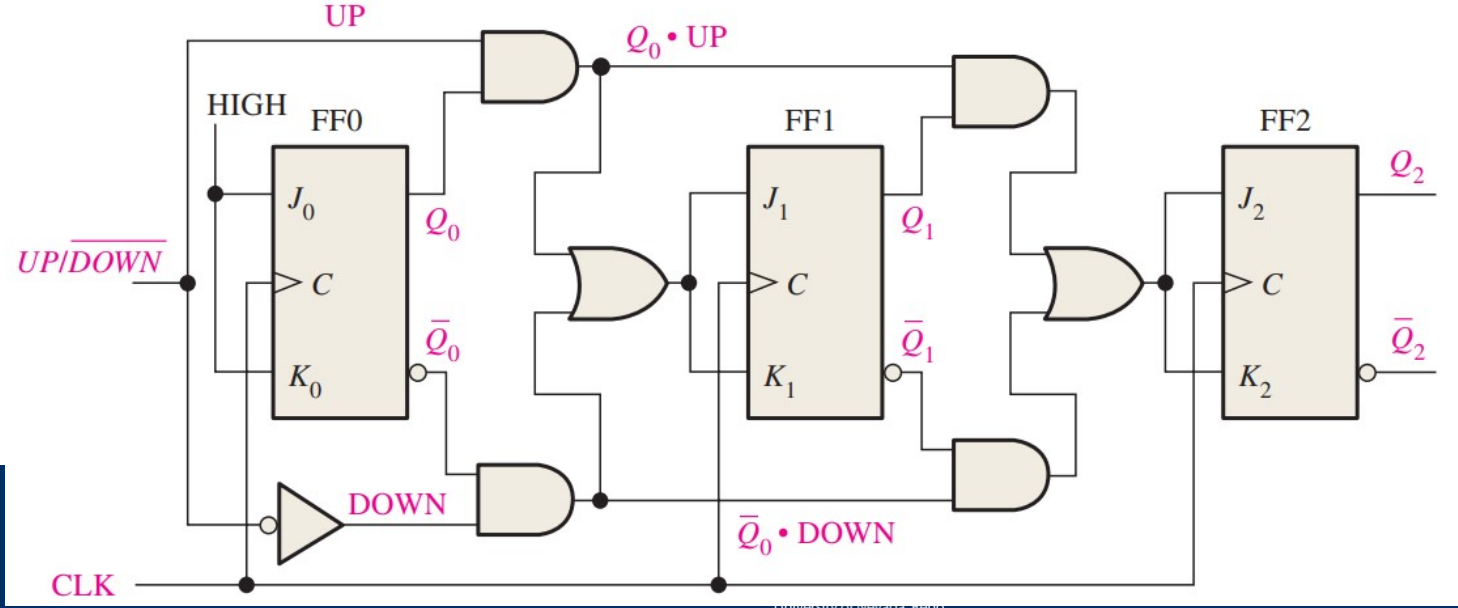
# Bidirectional Counter

- $J_0=K_0=1$
- $J_1=K_1=(Q_0 \bullet UP) + (Q_0' \bullet DOWN)$
- $J_2=K_2=(Q_0 \bullet Q_1 \bullet UP) + (Q_0' \bullet Q_1' \bullet DOWN)$

| Clock Pulse | Up | $Q_2$ | $Q_1$ | $Q_0$ | Down |
|---|---|---|---|---|---|
| 0 | ↻ | 0 | 0 | 0 | ↺ |
| 1 | ↻ | 0 | 0 | 1 | ↺ |
| 2 | ↻ | 0 | 1 | 0 | ↺ |
| 3 | ↻ | 0 | 1 | 1 | ↺ |
| 4 | ↻ | 1 | 0 | 0 | ↺ |
| 5 | ↻ | 1 | 0 | 1 | ↺ |
| 6 | ↻ | 1 | 1 | 0 | ↺ |
| 7 | ↻ | 1 | 1 | 1 | ↺ |

# Bidirectional Counter

- Copy and paste FF1 and circuitry to extend



# Reading

- This lecture
  - Sections 9.1-9.4
- Next lecture
  - Sections 9.5-9.10